Semiconductor Technology from A to Z

Assembly

Dicing

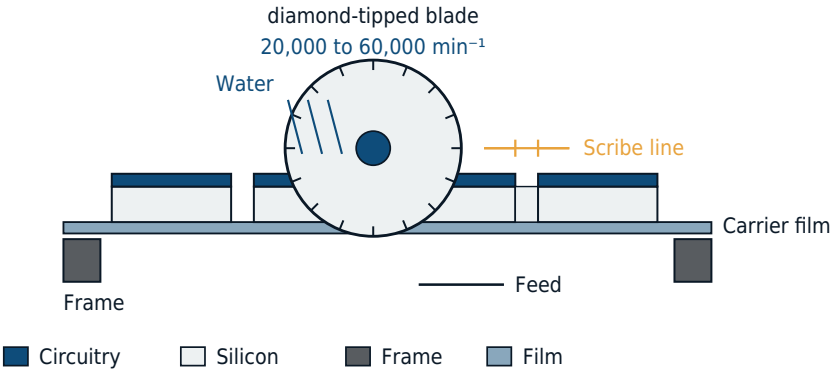
From Wafer to Individual Chip

After the wafer test, the wafer still exists as a single, continuous disc containing hundreds to several thousand individual dies, separated by narrow, unpopulated strips – the so-called scribe lines or dicing lanes. These strips contain no functional circuit structures and are deliberately reserved for the subsequent separation step.

During dicing (also called wafer sawing or die separation), the wafer is cut into individual dies along these scribe lines. This step marks the transition from the front-end of manufacturing, where all dies were still processed together on the wafer, to the back-end, where each die is handled individually from this point onward.

Dicing – Sawing the Wafer

The saw cuts along the scribe lines, the film holds the dies



The scribe lines carry no circuitry – their width limits how thick the blade can be. As they get narrower with miniaturization, laser methods are gaining importance. The film keeps the dies in place after cutting.

Before the actual separation, the wafer is typically mounted onto a thin, elastic carrier film (dicing tape) stretched over a metal frame. This film keeps the individual dies in their original position after sawing, preserving the spatial correspondence to the previously generated yield map.

Sawing Methods

The most widely used method is mechanical sawing with a thin, diamond-

embedded circular blade (blade dicing). The blade rotates at very high speed (typically 20,000 to 60,000 revolutions per minute) and is continuously cooled and flushed with deionized water during cutting to dissipate frictional heat and remove sawing debris from the cut.

The width of the scribe lines limits how narrow the saw blade can be and how precisely the cut must be guided. As available scribe line width continues to shrink with ongoing miniaturization, alternative separation methods are gaining increasing importance:

- Laser dicing: a focused laser beam separates the wafer either by direct ablation of material or by deliberately introducing internal micro-cracks (stealth dicing), along which the wafer is subsequently broken apart mechanically
- Plasma dicing: the wafer is completely etched through along the scribe lines using an anisotropic dry etch process; this method produces particularly smooth, damage-free edges and is well suited for very thin wafers

Each method has specific advantages and disadvantages regarding cutting speed, mechanical stress on the material, and achievable edge quality, which is why the choice of separation method depends on the specific product and wafer layer stack.

Challenges and Quality Assurance

During mechanical sawing, fine chipping can occur at the edge of the cut – small fractures of the brittle silicon material. These micro-cracks can propagate further under mechanical or thermal stress during the component later operation, potentially compromising reliability. Sawing parameters – particularly feed speed, rotational speed and cooling – must therefore be carefully matched to the specific layer system of the wafer.

Particular challenges arise with wafers containing sensitive layer stacks, such as components with low-k dielectrics in the wiring layers. These porous materials are considerably more mechanically fragile than classic silicon dioxide and are more prone to delamination – the separation of individual layers – during sawing.

After separation, the quality of the cut edges is frequently inspected optically. In addition, the previously generated yield map remains valid: since the dies remain in position thanks to the carrier film, the map can be used to unambiguously determine which of the now-separated dies were already identified as functional during the wafer test, and therefore proceed to the next assembly step, die attach.

Die Attach

Mechanical Mounting of the Die

After dicing, the individual, already identified functional dies remain on the carrier film. In the first step of the actual assembly process, each die is lifted from the film (die pick) and mechanically mounted onto its final carrier material – this process is referred to as die attach or die bonding.

Depending on the component type, different carrier materials (substrates) are used:

- Leadframe: a stamped or etched metal grid, usually made of copper or a copper alloy, which later forms the outer leads of the package
- Laminate or ceramic substrate: multilayer carrier boards with integrated wiring, as used for example in ball-grid-array packages (BGA)
- Direct chip attach: in some applications, the die is mounted directly onto a printed circuit board or another system without first receiving its own package

The die is precisely picked up by a gripping tool (die bonder), aligned, and placed onto the substrate with a defined contact force. Accurate positioning is important, since in the subsequent bonding step the die contact pads must line up as closely as possible with the corresponding connection points on the substrate.

Bonding Materials

Various materials are used to actually attach the die to the substrate, with the choice depending on the electrical, thermal and mechanical requirements of the specific component:

- Adhesives (epoxy resins): by far the most commonly used method. The adhesive is either dispensed as a paste or applied in pre-formed film form (die attach film) between die and substrate, and subsequently cured thermally. Electrically conductive adhesives additionally contain fine silver particles to establish, in addition to the mechanical bond, an electrical connection between the backside of the die and the substrate
- Solder joints: particularly for components with high heat dissipation requirements, such as power semiconductors, the die is bonded directly to the substrate using a solder material (often gold- or tin-based). Solder joints offer significantly better thermal conductivity than adhesives
- Eutectic bonding: the die is bonded directly to a thin eutectic metal layer (frequently a gold-silicon alloy) on the substrate under the application of

heat, without requiring an additional paste-form bonding material

The choice of bonding material significantly influences how efficiently the heat generated by the chip during operation can be dissipated through the substrate – a particularly critical factor for high-performance processors and power semiconductors.

Mechanical Stress and Quality Assurance

A key challenge in die attach is mechanical stress arising from differing thermal expansion coefficients between die and substrate. Silicon and common substrate materials such as copper or ceramic expand to different degrees with temperature changes. During curing of the bonding material, and later during operation of the finished component, this can generate stress within the die that, in the worst case, leads to cracking.

To limit this stress, bonding materials with a certain degree of elasticity are used, capable of compensating for small expansion differences without damaging either the bond itself or the die. In addition, the thickness of the bonding material layer is carefully controlled: a layer that is too thin provides insufficient compliance, while a layer that is too thick can worsen the thermal connection.

After the bonding material has cured, the quality of the die attach bond is inspected, among other things through optical inspection for voids (cavities within the bonding material) and through shear strength testing, in which the mechanical adhesion of the die is checked on a sample basis. Only after successful inspection does the die proceed to the next process step, bonding.

Bonding

Electrical Contacting of the Die

After the die has been mechanically attached to the substrate through die attach, it still needs to be electrically connected to the substrate connection structures. This process is referred to as bonding. Electrical contacting is achieved in about 90% of cases via wire bonding, while the mechanical attachment of the chip – as described in the previous chapter – is mainly carried out by bonding with epoxy resins.

In wire bonding, thin wires made of gold or aluminum are used, which are cold-welded to the contact pads of both chip and substrate. Three common variants

are distinguished:

- Thermosonic ball-wedge bonding
- Ultrasonic wedge-wedge bonding
- Thermocompression ball-wedge bonding

In all three methods, a small ball first forms at the end of the wire, created by locally melting the wire tip. Due to the strong surface forces of the molten gold, the melt solidifies into a ball whose larger diameter compared to the bond wire ensures a more reliable mechanical and electrical connection.

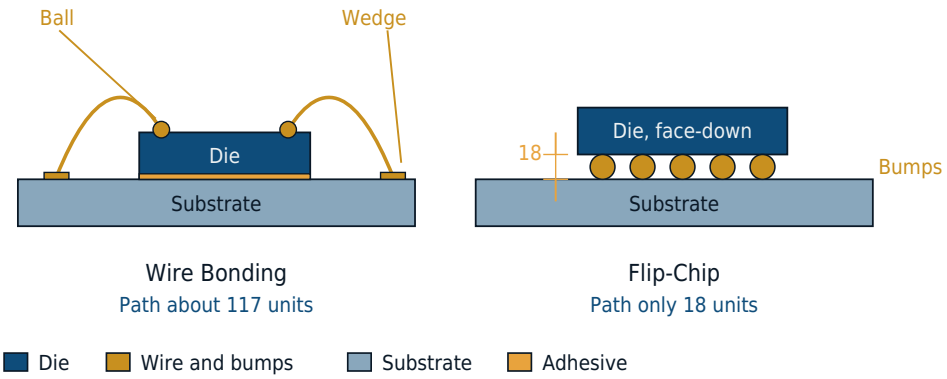
Flip-Chip Technology

In addition to classic wire bonding, flip-chip technology offers an alternative method that requires no long bond wires at all and represents the most compact form of connection between chip and substrate.

To create a flip-chip connection, small solder bumps must be present on the chip and/or the substrate. To form the connection, the chip is placed face-down, but with very precise alignment, onto the substrate. During a subsequent reflow process, the bumps melt and simultaneously form a mechanical and electrical connection between chip and substrate.

Wire Bonding and Flip-Chip

The length of the connection path determines inductance and heat



The bond wire is roughly 6 times as long as the path across a bump. Short paths mean less parasitic inductance and better heat dissipation – both favor flip-chip technology.

The key advantage of flip-chip technology lies in the very short connection paths from chip to substrate via the solder bumps – in contrast to the comparatively

long wire bonds used in classic wire bonding. This reduces parasitic inductance and capacitance in the connection, which is electrically advantageous at very high signal frequencies.

Since a flip-chip connection typically leaves an air gap between chip and substrate, it is usually necessary to additionally introduce a so-called underfiller. This fills the remaining gap between chip and substrate and compensates for mechanical stress arising from the differing thermal expansion coefficients of the two materials.

Requirements and Heat Dissipation

Regardless of the bonding method chosen, the electrical connections between chip and substrate must meet a number of fundamental requirements: low electrical resistance, high reliability over the component entire service life, and good mechanical adhesion even under thermal cycling.

An increasingly important aspect of bonding is heat dissipation. As the power dissipation of modern chips continues to rise, removing the resulting heat becomes a very important consideration throughout the entire packaging and interconnection process. Short conduction paths and materials with good thermal conductivity are indispensable for this. This is precisely where flip-chip technology offers advantages over classic wire bonding, since the short connection paths via the bumps are also more favorable for heat dissipation than long bond wires.

Once bonding is complete, the chip is fully electrically connected to its substrate. The next step in assembly is to protect this sensitive connection, as well as the die itself, from external influences through suitable encapsulation.

Encapsulation

Purposes of Encapsulation

After bonding, the die is fully electrically connected to its substrate but still lies exposed and unprotected. In the final major step of assembly, the die is therefore embedded in a protective molding compound – this process is referred to as encapsulation or molding.

As part of the overall packaging process, encapsulation fulfills several fundamental purposes:

- Protecting the circuit from external influences such as moisture, dust and

mechanical damage
- Routing the sensitive on-chip contacts out to robust, manageable external connections
- Supplying the circuit with electrical power via the package leads
- Dissipating the power loss generated during operation
- Distributing signals and data between the chip and the surrounding circuitry

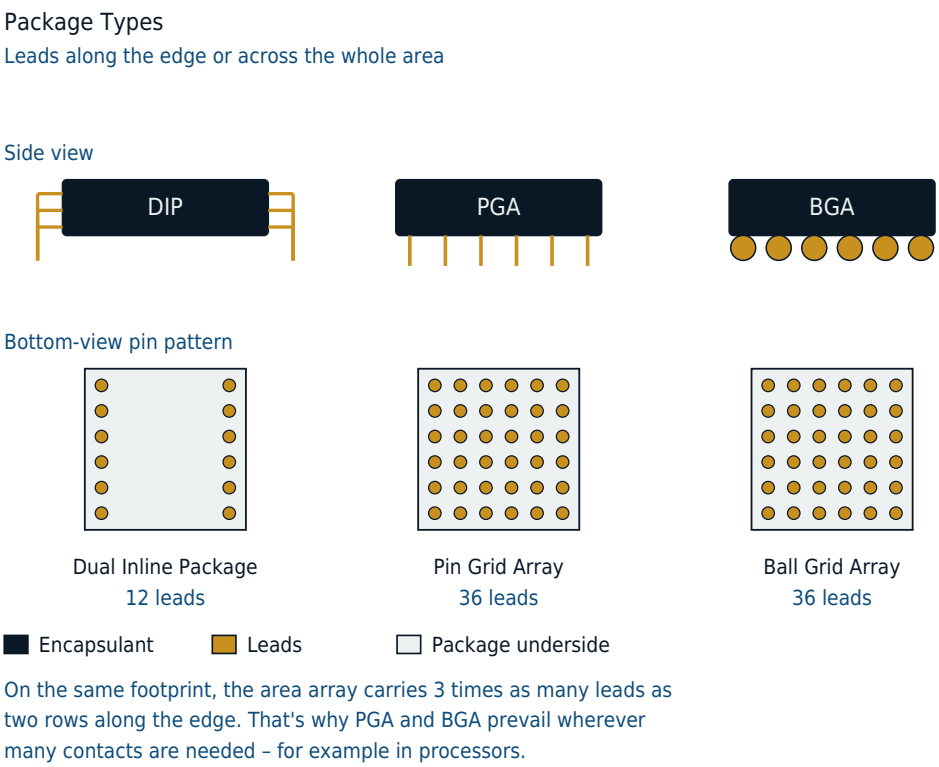
The trend in packaging technology is toward increasingly smaller and thinner packages (chip size package, CSP), in which the finished package is only marginally larger in length and width than the actual chip, typically by a factor of around 1.2.

Materials and Methods

The most widely used method is molding, in which the die, together with its bond wires or bumps, is injected into a thermoset plastic compound. This molding compound cures under heat and subsequently forms the actual, solid package of the component.

Well-known package types produced this way include, for example:

- DIP – Dual Inline Package
- PGA – Pin Grid Array, commonly used especially for processors
- BGA – Ball Grid Array



For components with particularly high heat dissipation requirements, such as power semiconductors, packages made from highly thermally conductive materials such as metal or ceramic are used instead of plastic. However, these materials are considerably more expensive than plastic, which is why mass production predominantly relies on plastic packages.

In the flip-chip technology described earlier, a classic full package is often omitted entirely: here, the underfiller already introduced during the bonding step takes over part of the protective function, while the chip itself remains exposed on the substrate.

Heat Dissipation and Final Quality Inspection

As the power dissipation of modern chips continues to increase, heat dissipation is one of the most important considerations when selecting package type and molding material. Short conduction paths and materials with good thermal conductivity are indispensable for this. For particularly high-performance components, additional heat dissipation measures are therefore frequently integrated into the package design, such as exposed metal areas on the underside of the package (exposed die pad) or dedicated thermal paths within the substrate.

After the molding compound has cured, the package is given a unique marking, typically via laser engraving, which carries manufacturer information, type designation and, where applicable, the result of the preceding binning step.

This concludes the actual assembly process. The fully encapsulated chip subsequently undergoes the final functional test described earlier, before being packaged for shipment to device manufacturers.