Semiconductor Technology from A to Z

Digital technology

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Circuit Layouts

From Schematic to Layout

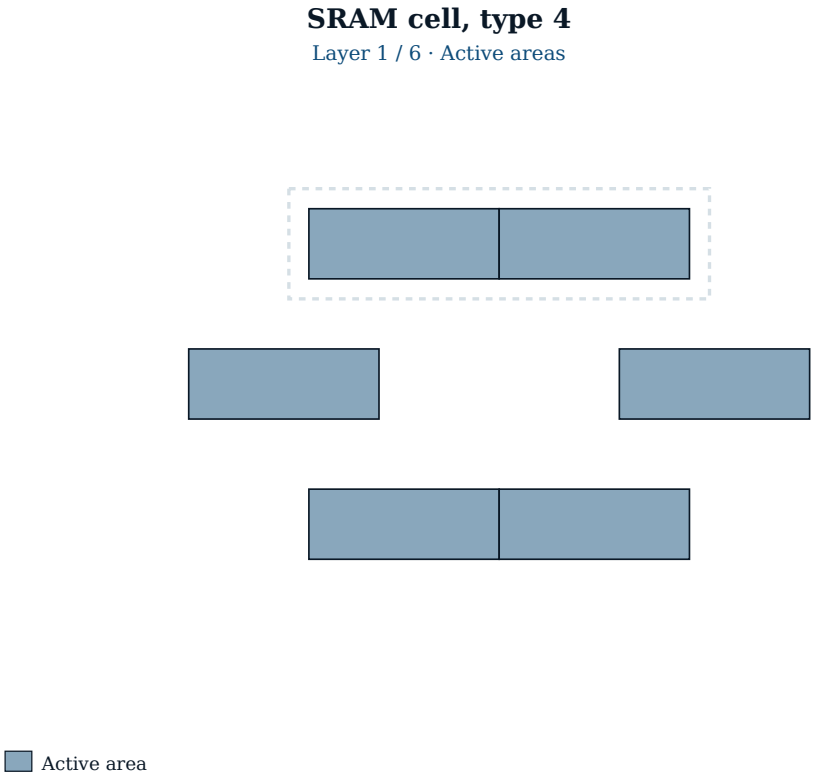
The schematic from the previous chapter shows *how* the six transistors are electrically connected. But it says nothing about *where* in the chip these transistors actually sit, or how the connections between them are manufactured. That's exactly what the layout shows: the sequence of masks used to expose and pattern each fabrication layer — diffusion, polysilicon, contacts, and no fewer than three metal layers.

This cell follows a common style often called "type 4": the two storage nodes Data and Data_b run as continuous columns from the top (PMOS) through the middle (access transistors) to the bottom (NMOS), spanning the full cell height. VDD sits centrally between the two columns, BL and BL̄ on the outside, VSS at the top and bottom, and the word line (WL) runs across the middle.

Symbol	Meaning
VDD	supply voltage (central, vertical)
VSS	ground (top and bottom, horizontal)
BL / BL̄	bit line / inverted bit line (outside, vertical)
WL	word line (middle, horizontal)
Data / Data_b	the two cross-coupled storage nodes
PU	pull-up transistor (PMOS, pulls toward VDD)
PD	pull-down transistor (NMOS, pulls toward VSS)

Layer 1: Active Areas

Six rectangles in three rows: the two PMOS (pull-up, in the N-well) on top, the two access transistors in the middle, and the two NMOS (pull-down) at the bottom. Each column — "Data" on the left, "Data_b" on the right — runs as its own active area through all three rows. That's the core idea of the type-4 layout: an inverter isn't made of two transistors side by side, but of a PMOS on top and an NMOS at the bottom *in the same column*, with the access transistor in between.



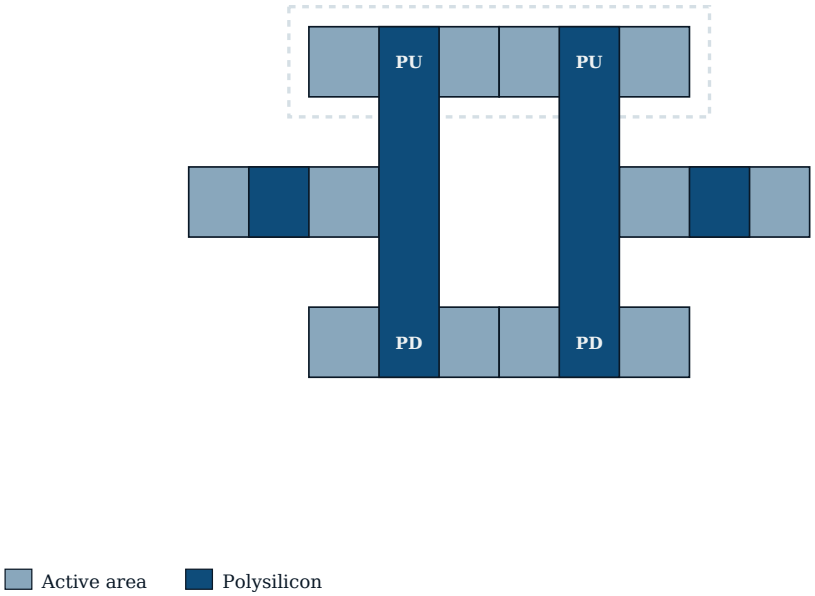
Layer 2: Polysilicon

Two continuous vertical gates are added — gate A (which later drives the Data node, though note: its *own* gate signal is Data_b, see below) and gate B, each running from the PMOS row down to the NMOS row. The two access transistors, in contrast, only get short, local gate stubs — no continuous polysilicon word line. The reason: a continuous poly WL would run straight through gate A and gate B and short them together. WL is instead added in layer 6 as a metal line, sitting one layer higher and therefore crossing over the gates without conflict.

Important for the cross-coupling: the pull-up/pull-down pair of one column is always driven *by the other column* — Data-side transistors are gated by Data_b, and Data_b-side transistors are gated by Data. Otherwise an inverter would be driving its own output, and the cell couldn't hold a bit.

SRAM cell, type 4

Layer 2 / 6 · + polysilicon

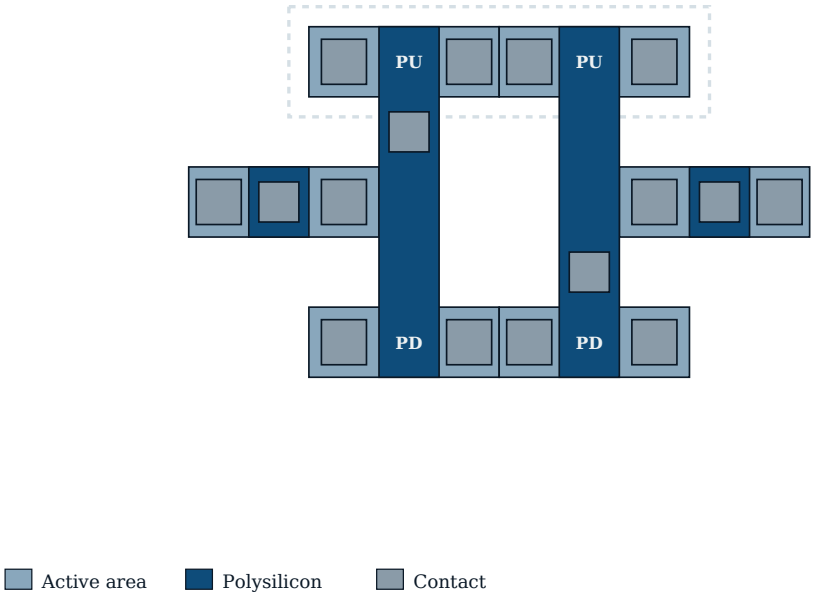


Layer 3: Contacts

Contact squares appear everywhere the next layer (metal-1) needs electrical access to diffusion or polysilicon: at both ends of every Data/Data_b column (PMOS drain, access-transistor drain, NMOS drain), at the source connections (VDD, VSS, BL, BL), and one each on gate A and gate B for the feedback path.

SRAM cell, type 4

Layer 3 / 6 · + contacts



Layer 4: Metal-1

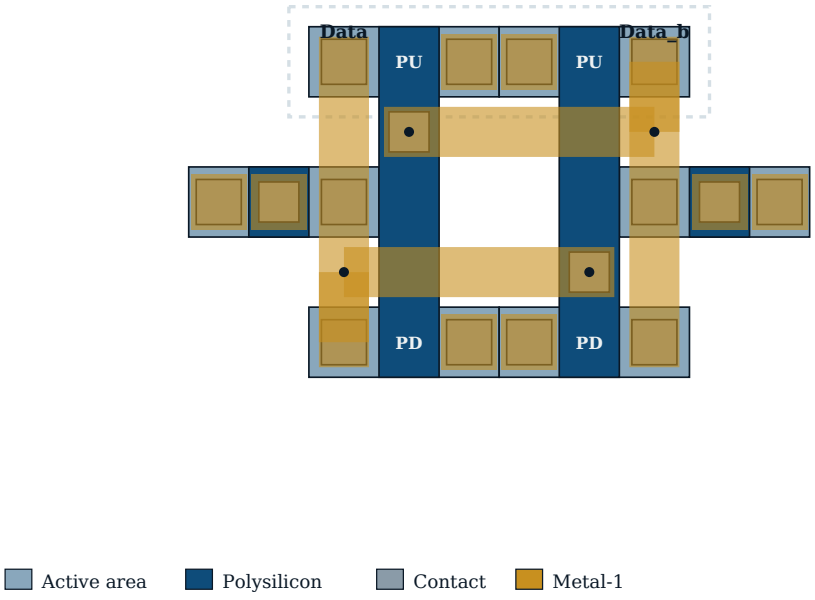
This is where the actual wiring inside the cell happens. Two things at once:

First, the local connection: each Data/Data_b column gets a continuous metal-1 trace that ties the PMOS drain, access-transistor terminal, and NMOS drain together into a single electrical node.

Second, the feedback across the full cell height: Data_b has to reach gate A, and Data has to reach gate B — both paths necessarily cross, but must never touch. This is solved by routing the two paths through different gaps (one above, one below the word-line row), so that in the picture they form an "O"-shaped loop around the two gates without ever crossing each other.

SRAM cell, type 4

Layer 4 / 6 · + metal-1

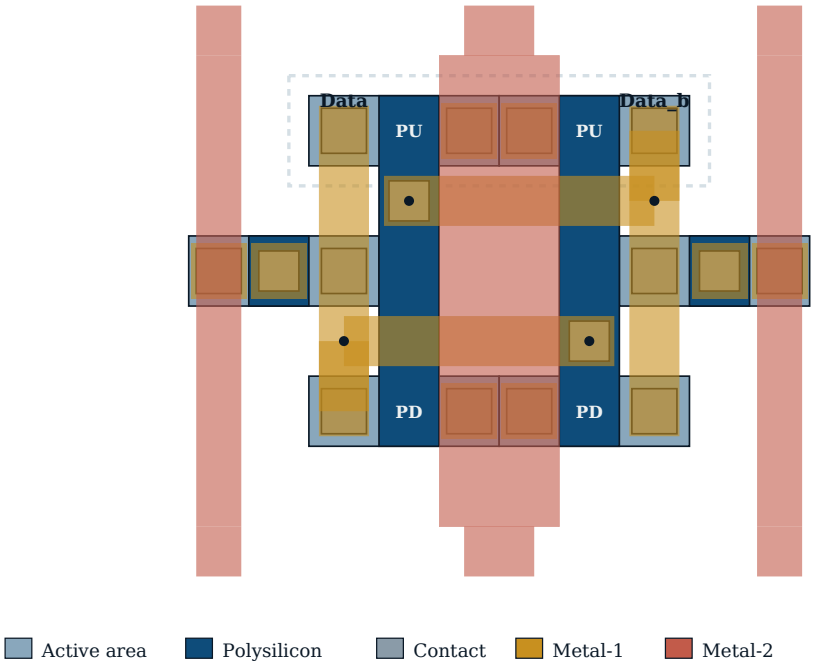


Layer 5: Metal-2

VDD, BL, and BL are added as vertical lines — VDD centrally between the two columns, BL and BL on the outside. All three run the full height of the cell and are ready at the top and bottom edges to connect to the next cell in the same column of the array.

SRAM cell, type 4

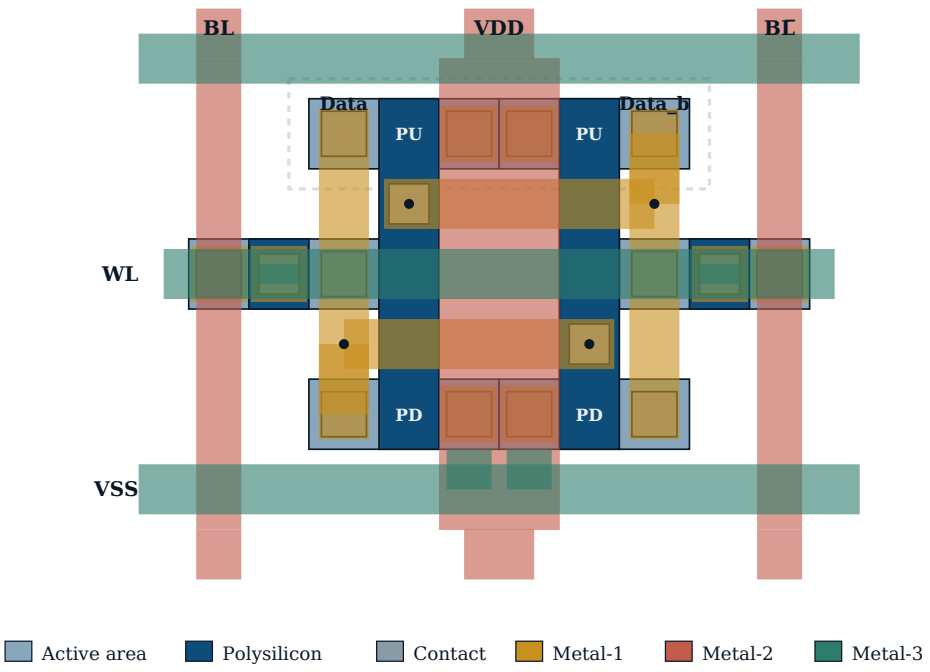
Layer 5 / 6 · + metal-2 (VDD, BL, BL̄)



Layer 6: Metal-3 — Complete

Finally, VSS (top and bottom) and WL (middle), both horizontal. That WL only appears here, instead of in polysilicon, is no accident: on this layer it can run freely over VDD, gate A, and gate B, because every layer beneath it is insulated underneath — crossings between *different* layers are unproblematic; only the *same* layer must never touch itself.

With that, the cell is fully wired. All four connections (VDD, VSS, BL, BL̄, WL) sit ready at the edges to connect seamlessly to neighbouring cells in the array — VDD/BL/BL̄ upward and downward (same column), VSS/WL left and right (same row).



A note on the rendering: from metal-1 onward, every layer is drawn semi-transparent rather than opaque — just like in real layout editors (e.g. Virtuoso, KLayout), where transparent layers let you see what lies underneath.