Semiconductor Technology from A to Z

Digital technology

DRAM Fabrication: The Trench Capacitor Process

General Structure and Operating Principle

The DRAM Memory Cell: One Transistor, One Capacitor

A DRAM cell (Dynamic Random Access Memory) stores a single bit as electrical charge on a capacitor. An access transistor connects this capacitor to the bitline on demand — while the transistor is off, the charge stays isolated and the bit remains stored; once switched on via the wordline, the charge can be read out or rewritten. This pairing of one transistor and one capacitor is called a 1T1C cell and is by far the most area-efficient way to store a bit — considerably more compact than the six transistors of an SRAM cell, but with one decisive drawback: the stored charge slowly leaks away and must be periodically refreshed every few milliseconds, hence the name "dynamic."

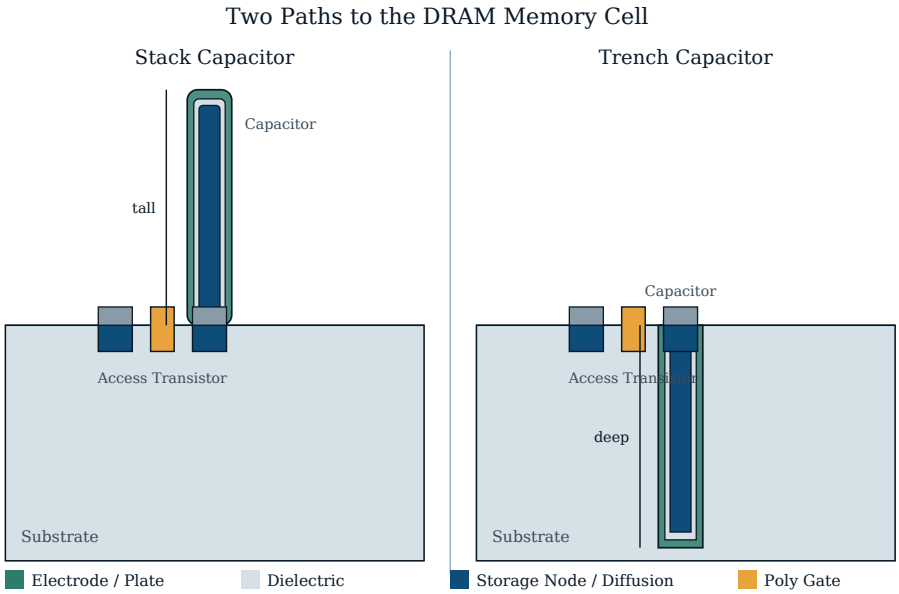
The challenge in cell design is purely geometric: a capacitor needs area to store enough charge for a reliably readable signal — typically on the order of a few femtofarads. Yet with every new technology node, the available cell area keeps shrinking while the required capacitance stays nearly constant. The manufacturing industry has solved this problem in two fundamentally different ways.

Two Paths to the Same Goal: Stack versus Trench

The stack capacitor (dominant at Samsung, SK Hynix, and Micron) builds the needed area vertically above the access transistor: cylindrical or crown-shaped electrode structures rise above the wafer surface and can, within the limits of lithography and etch technology, grow nearly arbitrarily tall.

The trench capacitor (historically developed by IBM and used at, among others, Infineon/Qimonda) instead pushes the same area downward: a deep, narrow trench is etched several micrometers into the substrate, with the capacitor electrodes forming concentric cylindrical surfaces along its walls. The key advantage of this approach lies in the process sequence: the trench — the most demanding and critical part of fabrication — is formed before the access transistor, so the transistor itself is built on top of an almost planar wafer surface, without having to overcome the tall topography of an already-completed stack capacitor.

The diagram below compares both capacitor types in cross-section, before the following sections build up the complete trench process step by step.



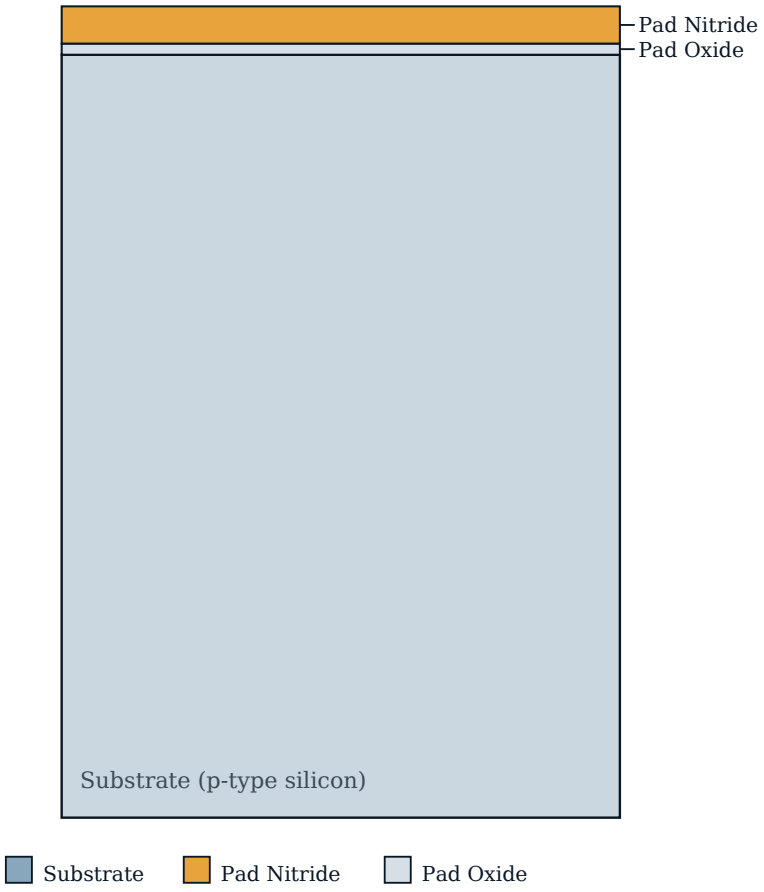
Trench Capacitor Fabrication

From Flat Wafer to Deep Trench

The trench capacitor process begins before a single transistor exists — the trench is etched as the very first structure into the still completely unprocessed wafer. This ordering is no coincidence: the most demanding, most critical part of the entire cell fabrication is meant to take place on a perfectly flat surface, unobstructed by any transistor or interconnect structures that would otherwise already be present.

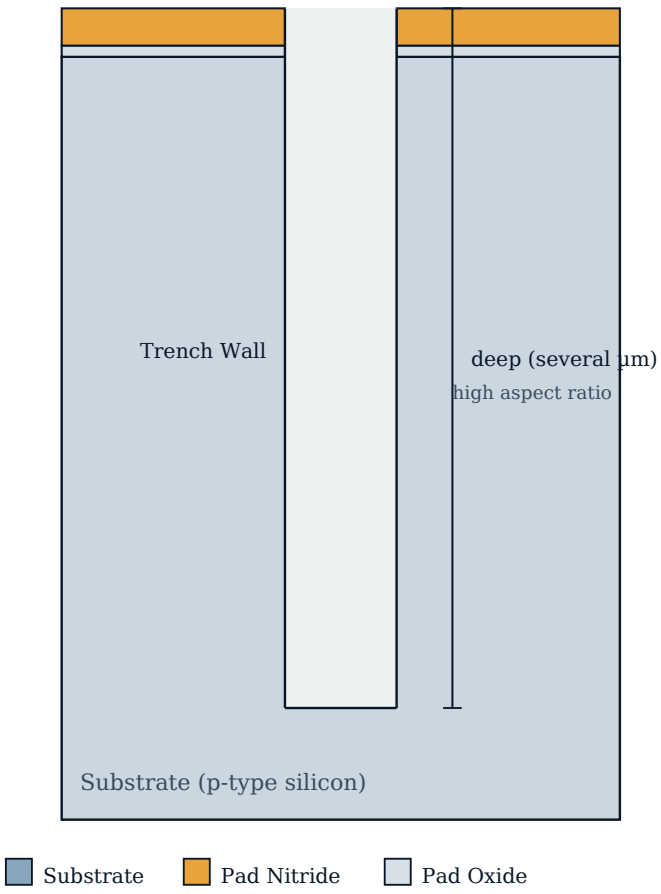
Step 1 – Pad Oxide and Pad Nitride: A thin thermal oxide layer (pad oxide) is first grown on the p-type silicon substrate, acting as a buffer that relieves mechanical stress between the substrate and the nitride layer that follows. Directly above it, a considerably thicker layer of silicon nitride (pad nitride) is deposited. This layer stack serves as the hard mask for the trench etch in the next step, and must be patterned to expose an opening only at the intended trench location.

Step 1: Pad Oxide and Pad Nitride



Step 2 – Deep Trench Etch: Through the opened hard mask, a highly anisotropic RIE process etches a narrow trench several micrometers deep into the substrate. The aspect ratio (depth to width) in modern trench cells is typically 50:1 or higher — one of the most demanding etch tasks in all of semiconductor manufacturing, since the sidewalls must remain uniformly vertical and smooth across the entire depth.

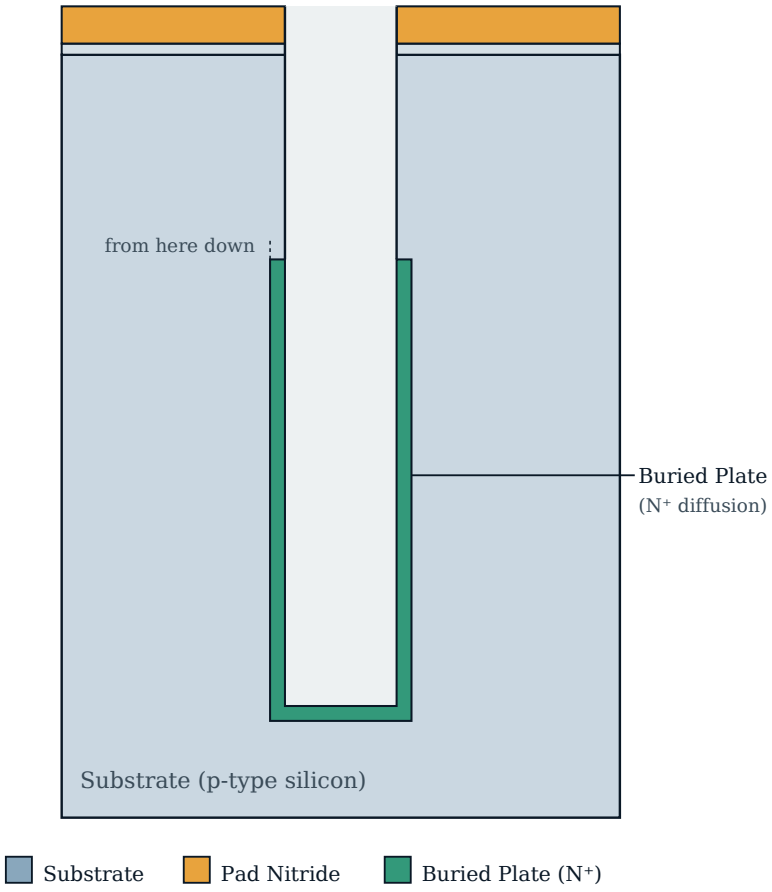
Step 2: Deep Trench Etch



The Capacitor Electrodes Take Shape

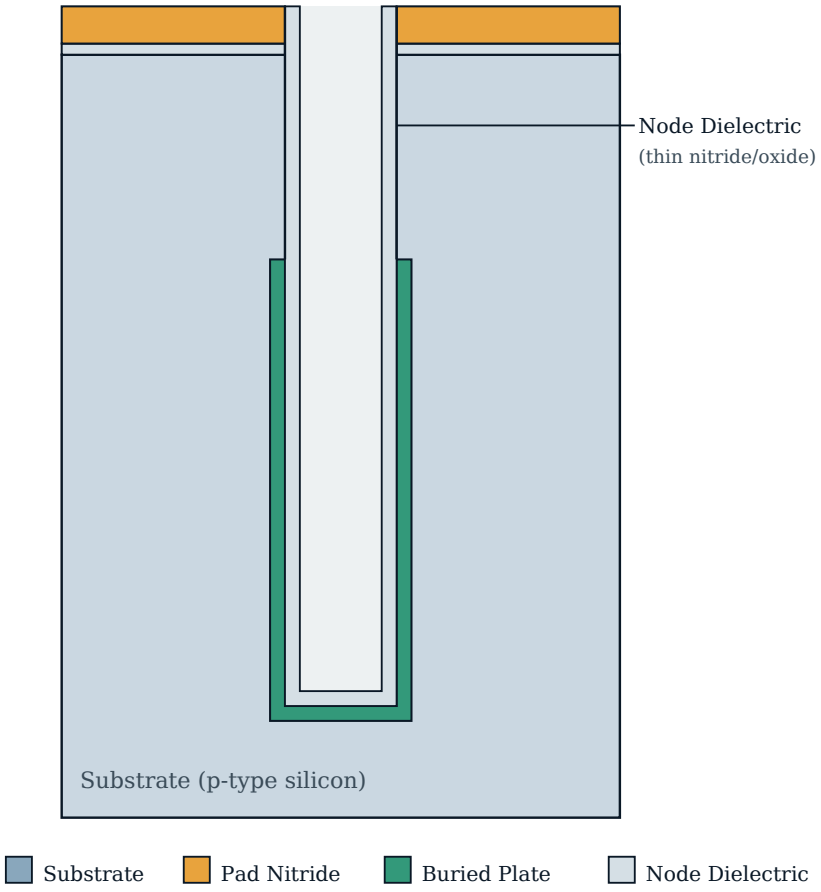
Step 3 – Buried Plate: The lower, deeper region of the trench wall is coated with an arsenic-doped glass layer, from which the dopant drives into the adjacent silicon wall at elevated temperature. This forms the buried plate — a heavily n-doped zone that serves as the outer capacitor electrode, shared in common by every cell in an array (comparable to the "ground plate" of a classic capacitor).

Step 3: Buried Plate



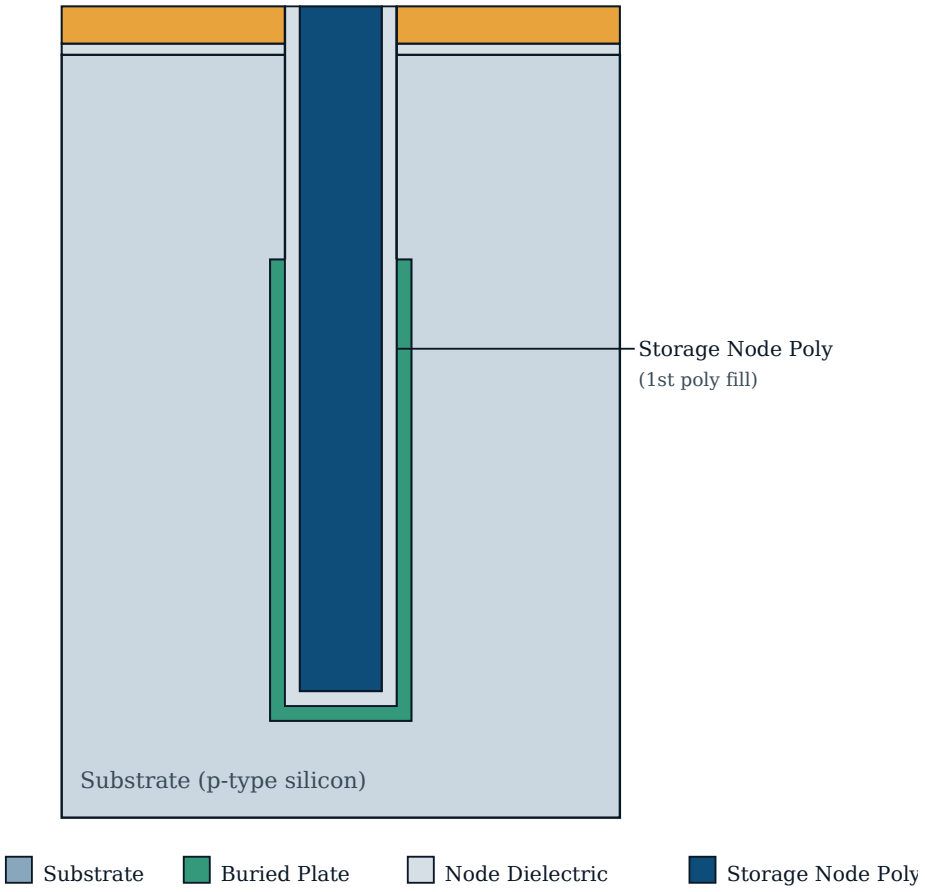
Step 4 – Node Dielectric: A conformal dielectric layer only a few nanometers thick — usually a nitride-oxide stack — is now deposited across the full trench depth. It separates the inner electrode that follows in the next step from the buried plate, and together with the trench wall area, largely determines the achievable capacitance of the cell.

Step 4: Node Dielectric



Step 5 – First Poly Fill: Doped polysilicon completely fills the remaining trench. This "storage node poly," together with the node dielectric and the buried plate, forms the actual capacitor: the charge stored on the poly represents the state of the stored bit.

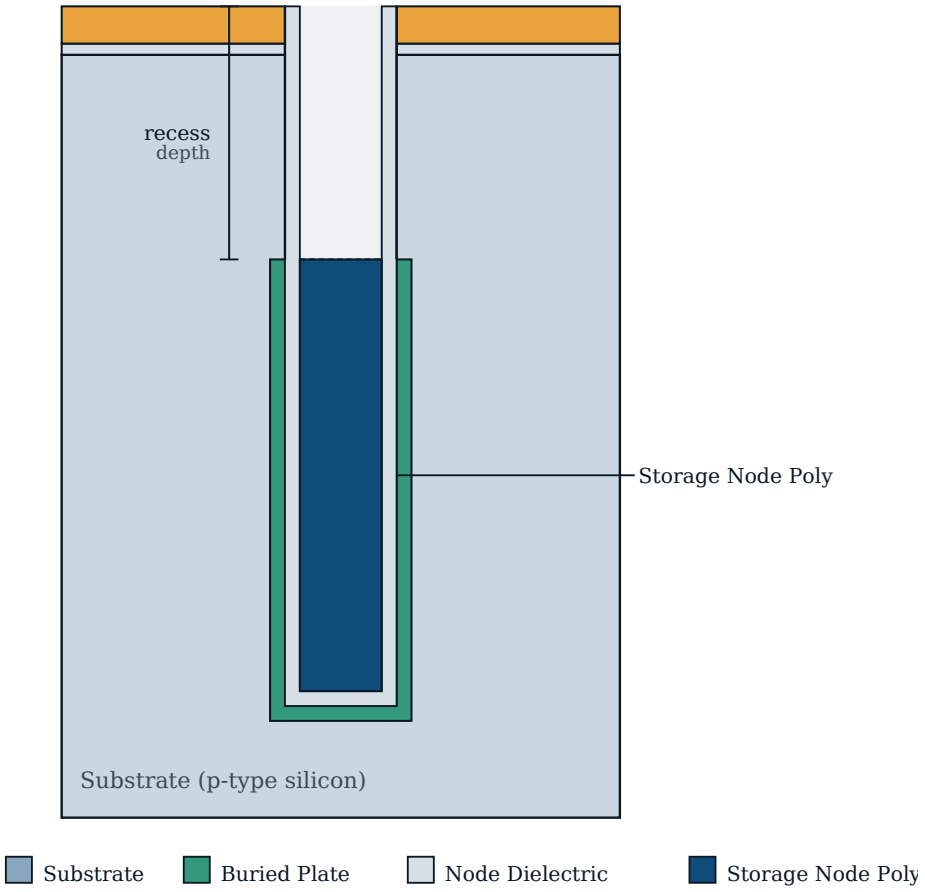
Step 5: First Poly Fill



The Upper Trench Region: Collar and Buried Strap

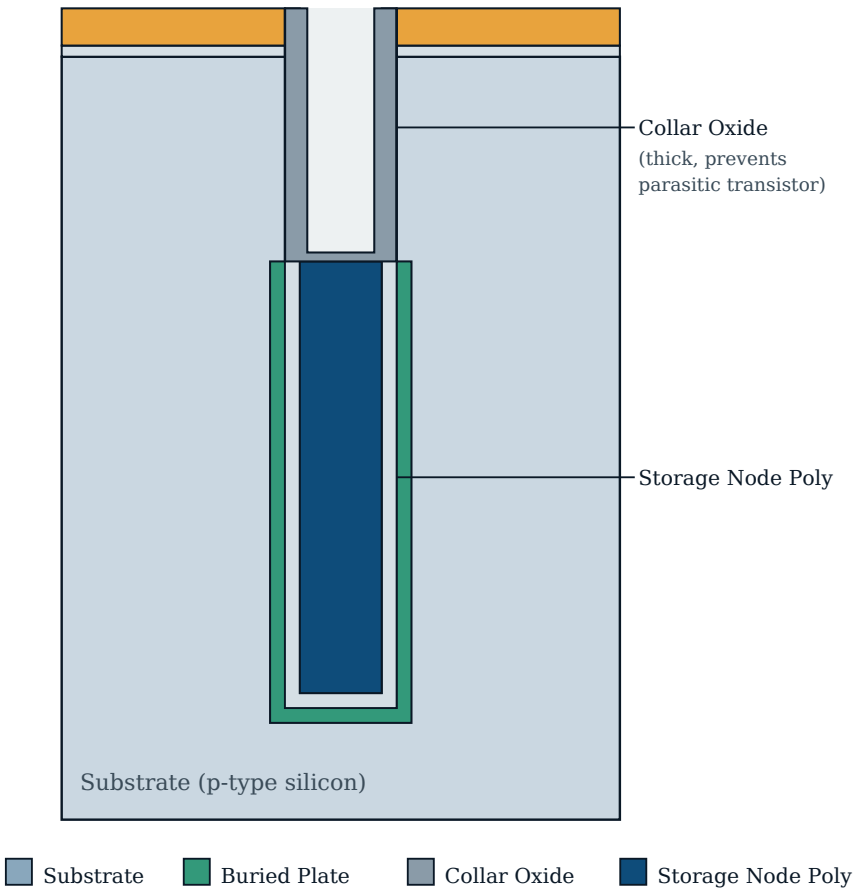
Step 6 – Poly Recess Etch: The storage node poly is selectively etched back so that it fills only the lower trench section surrounded by the buried plate. The upper trench region — where the access transistor will later sit directly beside the trench — is once again left open.

Step 6: Poly Recess Etch



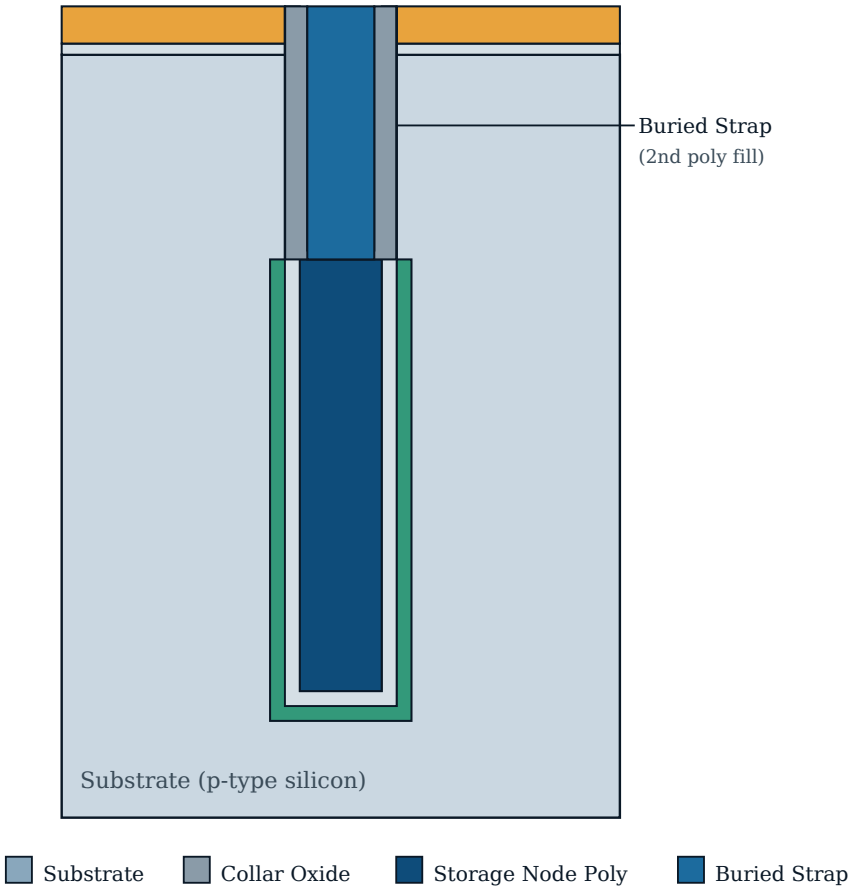
Step 7 – Collar Oxide: In the now-exposed upper trench section, the thin node dielectric is removed and replaced with a considerably thicker oxide layer, the collar. Without this thick oxide, the later wordline voltage could turn on a parasitic, unwanted transistor along the upper trench wall, letting charge leak past the actual access transistor. The collar reliably suppresses this leakage path.

Step 7: Collar Oxide



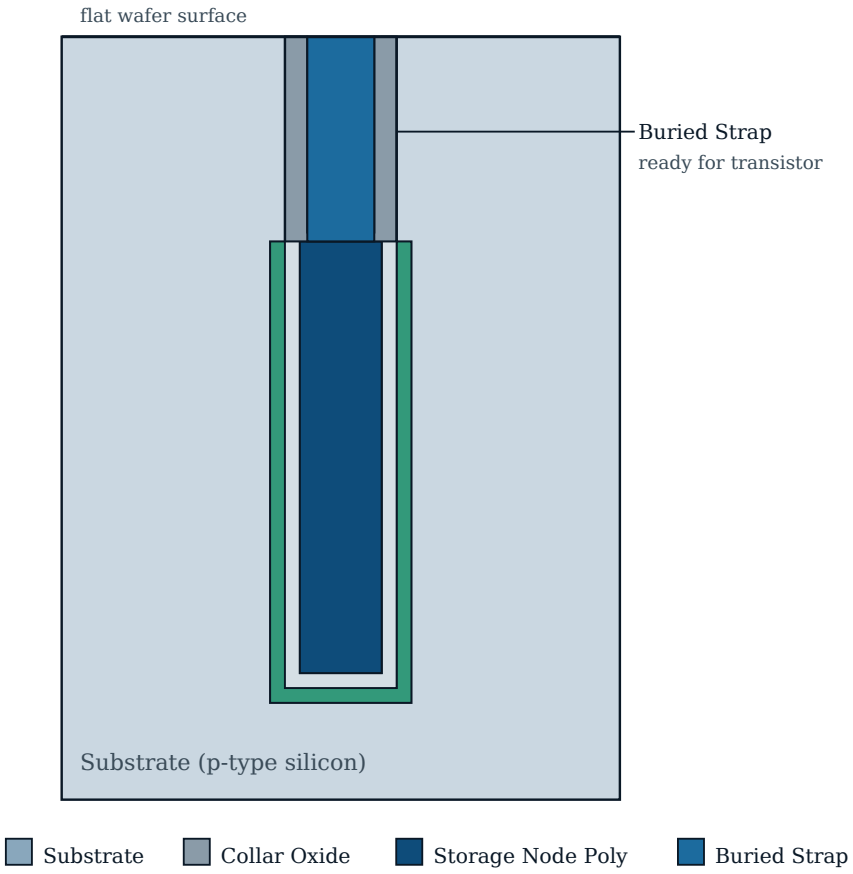
Step 8 – Buried Strap: A second polysilicon deposition completely fills the upper trench section, now narrowed by the collar. This so-called buried strap forms the electrical connection between the deep-lying storage node poly and the access transistor's future source/drain diffusion at the wafer surface — without it, the capacitor would remain electrically isolated from the transistor.

Step 8: Buried Strap



Step 9 – Planarization: A final CMP and etch step removes excess poly along with the entire pad-nitride/pad-oxide hard mask, restoring an almost flat wafer surface. The trench capacitor is now fully complete and, sitting flush with the substrate surface, awaits the access transistor — whose fabrication the next section describes.

Step 9: Planarization



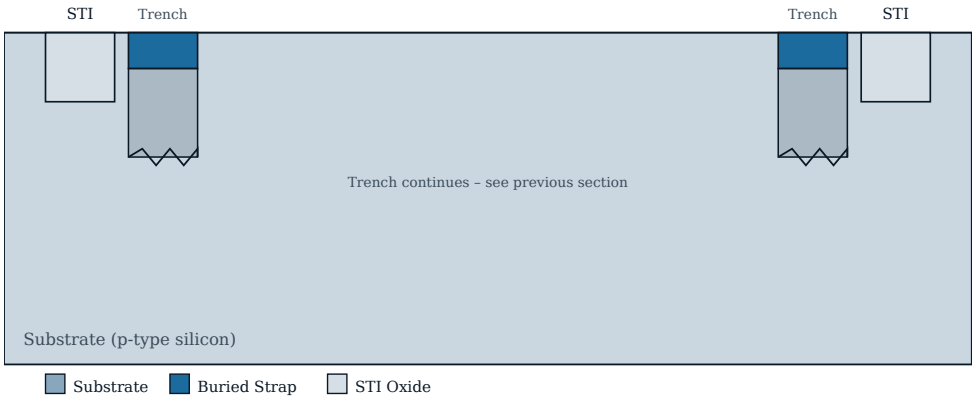
Access Transistor and Interconnect Fabrication

Two Cells, One Shared Bitline Contact

With the finished, planarized trench capacitor from the previous section, fabrication can continue where an ordinary logic process begins: on an almost flat wafer surface. The diagrams below show a typical cell pair — two neighboring trench capacitors whose access transistors share a common bitline contact in the middle. This "folded" arrangement saves one contact per two cells and is standard practice in trench DRAM fabrication.

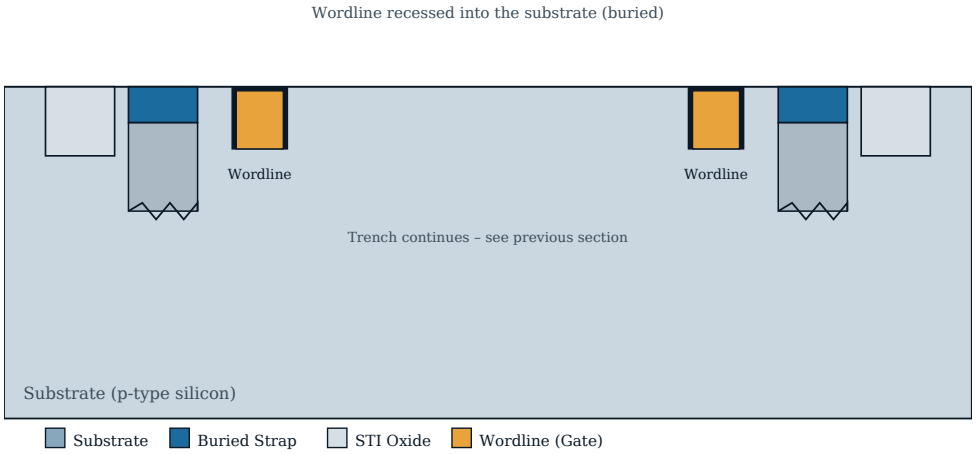
Step 10 – Shallow Trench Isolation (STI): At the outer edge of each cell pair, a shallow trench isolation separates that pair's active area from the next one's. Unlike the deep capacitor trench, the STI is only a few hundred nanometers deep and purely oxide-filled — it has no electrical function beyond separating neighboring devices.

Step 10: Shallow Trench Isolation (STI)



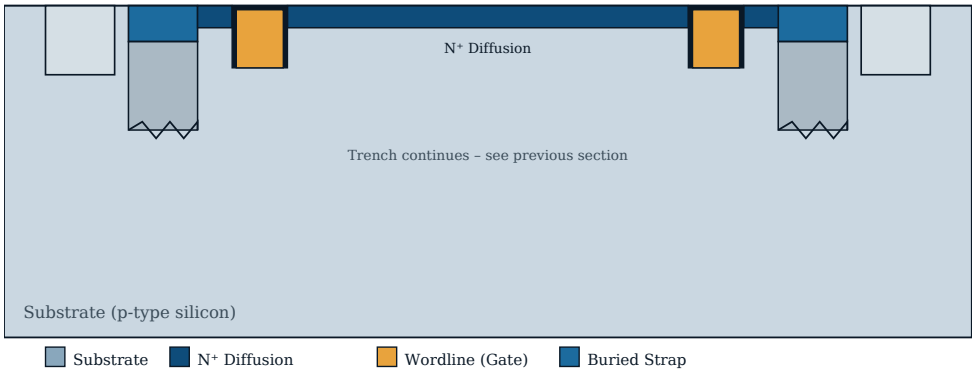
Step 11 – Gate Oxide and Buried Wordline: Between each trench and the future bitline contact, the access transistor is formed. Modern trench cells recess the wordline into a shallow pit in the substrate as a so-called buried wordline, lined with a thin gate oxide. This recessed structure does not shorten the effective channel while allowing a considerably more compact cell than a classic, surface-sitting gate electrode.

Step 11: Gate Oxide and Buried Wordline



Step 12 – Source/Drain Implantation: A shallow N^+ implant connects the active area continuously: from the left trench's buried strap, across the left wordline's channel to the center, onward across the right wordline's channel, to the right trench's buried strap. Each wordline thus switches the current path between "its" trench capacitor and the shared center node.

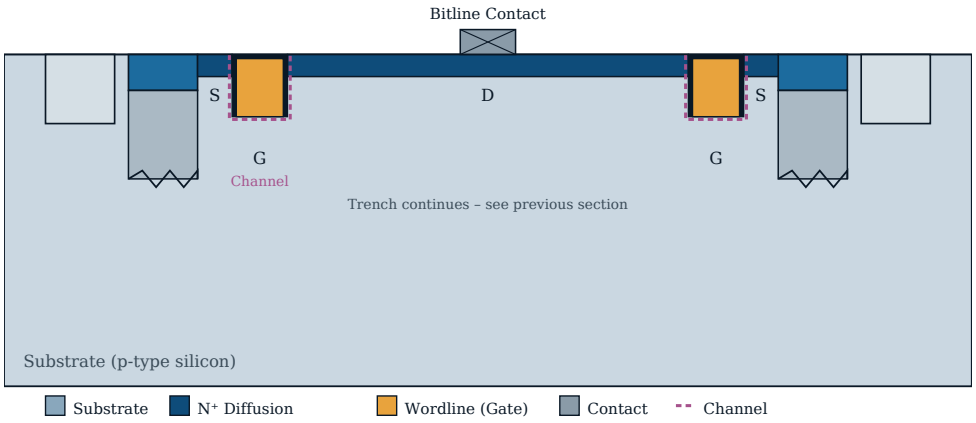
Step 12: Source/Drain Implantation



Connecting to the Interconnect Layers

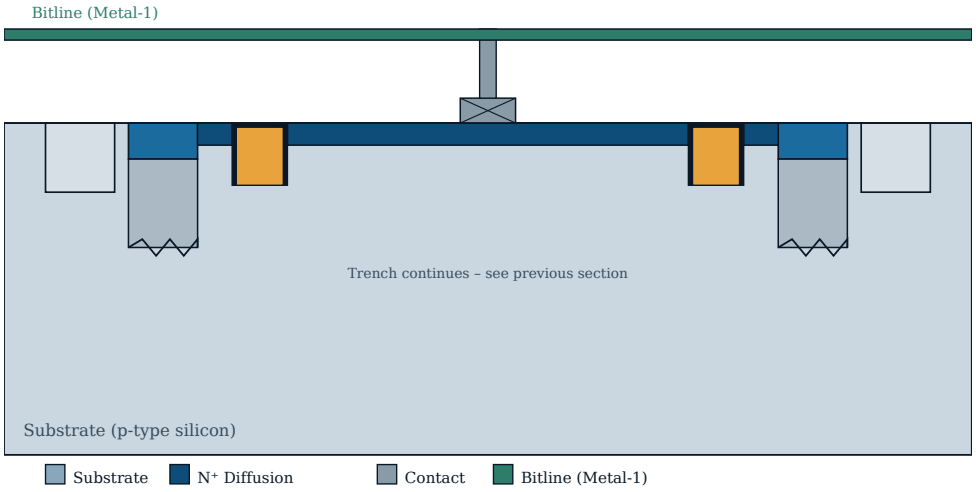
Step 13 – Bitline Contact: A contact hole is opened on the shared diffusion at the cell center and filled with metal. Through this single contact, both access transistors of the pair access the bitline together — hence the "folded" cell arrangement. The diagram uses this point to show, as an example, all three transistor terminals (G, S, D) along with the channel path: with a buried wordline, the channel does not form flat beneath the gate but wraps in a U-shape along the trench walls and floor — effectively lengthening the current path despite the compact cell area. Source and drain are shown here as fixed for clarity; electrically, both diffusion sides are symmetric and swap roles depending on the direction of operation.

Step 13: Bitline Contact



Step 14 – Bitline Metallization: The first metal layer (metal-1) wires the bitline contact into a continuous trace that runs across the entire cell array, connecting thousands of cell pairs in the same column. When reading a cell, a sense amplifier compares this bitline's voltage against a reference voltage to determine whether a "1" or "0" was stored.

Step 14: Bitline Metallization



Step 15 – Interlayer Dielectric and Contacts: An interlayer dielectric (ILD) embeds the bitline wiring while also providing the insulation for additional contacts — for instance the wordline connections outside the actual cell array, where the wordlines terminate in driver circuits. From here on, fabrication follows the same principles as any other logic process: further metal layers, vias, and contacts, as already described in the "Circuit Layouts" chapter. This completes the DRAM cell — from the deep capacitor trench to the connection into the first interconnect layer.

Step 15: Interlayer Dielectric and Contacts