

Semiconductor Technology from A to Z

Compound Semiconductors

Crystal Growth & Substrates	3
<i>SiC Crystal Growth: Physical Vapor Transport</i>	<i>3</i>
<i>Polytypes: Why 4H-SiC?</i>	<i>3</i>
<i>GaN Epitaxy: Heteroepitaxy Instead of Native Substrates</i>	<i>3</i>
<i>Lattice Matching, Strain and Defect Density</i>	<i>3</i>

Crystal Growth & Substrates

SiC Crystal Growth: Physical Vapor Transport

Unlike silicon, SiC cannot be pulled from a melt – at the temperatures required, SiC sublimes rather than melting. Instead, the PVT process (Physical Vapor Transport, also known as the modified Lely method) is used: a supply of SiC powder is heated above 2000 °C and sublimes, the vapor phase travels along a temperature gradient to a cooler SiC seed crystal and crystallizes there epitaxially. The process runs for days to weeks and grows a cylindrical boule, from which wafers are subsequently sawn.

Polytypes: Why 4H-SiC?

SiC occurs in more than 200 crystal structures (polytypes), which differ only in the stacking sequence of the Si-C double layers. 4H-SiC has become the standard for power electronics because it offers higher and more isotropic electron mobility than, for example, 6H-SiC. Growth is usually performed off-axis (typically a 4° miscut from the c-axis) to force step-flow growth during homoepitaxy and avoid polytype inclusions.

GaN Epitaxy: Heteroepitaxy Instead of Native Substrates

Native GaN substrates are expensive and available only in small diameters, because GaN does not melt congruently at normal pressure. In practice, GaN is therefore deposited heteroepitaxially on foreign substrates – usually silicon (GaN-on-Si, low cost, large diameters up to 200 mm) or silicon carbide (GaN-on-SiC, better heat dissipation, but more expensive). A thin AlN nucleation layer along with step-graded AlGaN buffer layers absorb the lattice and thermal expansion mismatch before the actual GaN layer grows.

Lattice Matching, Strain and Defect Density

The lattice constants of GaN and silicon differ by about 17%, and their thermal expansion coefficients by more than 50% – without buffer layers, the GaN layer would crack on cooling. Even with a buffer strategy, a significant dislocation density remains (typically 10^8 – 10^9 cm⁻² for GaN-on-Si, versus 10^3 – 10^4 cm⁻² for native SiC substrates). This explains the industry trade-off: GaN-on-Si for cost- and area-driven applications, GaN-on-SiC or native SiC substrates where reliability and thermal management take priority.