Semiconductor Technology from A to Z

Compound Semiconductors

SiC Power Devices

The SiC Power MOSFET

The SiC power MOSFET adopts the planar DMOS base structure of its silicon counterpart (see the fundamentals chapter "The MOSFET"), but exploits the much higher breakdown field strength of SiC to make the drift region significantly thinner and more highly doped at the same blocking voltage. This lowers the specific on-resistance R_on·A by more than an order of magnitude compared to an equivalent Si MOSFET – while simultaneously allowing a higher blocking voltage (600 V to over 3.3 kV) and a noticeably smaller chip area per ampere.

The SiC Schottky Diode

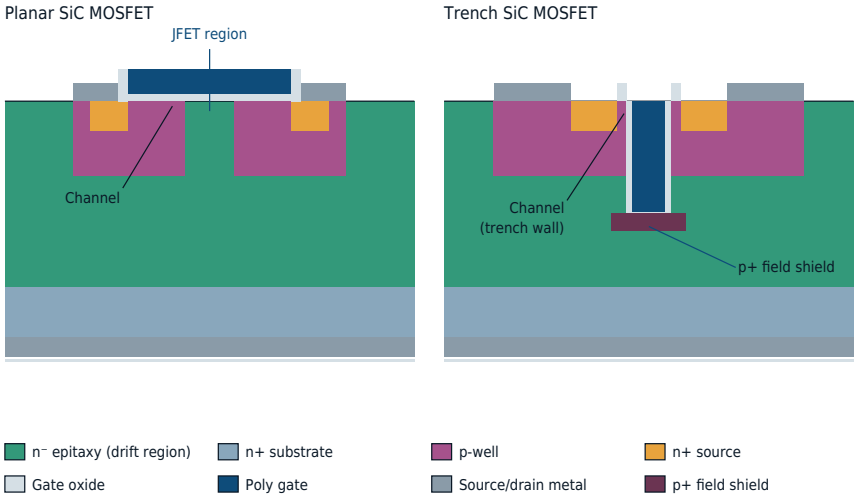
A Si pn diode needs time when switching off to clear the minority charge stored during conduction – the so-called reverse recovery time, which causes switching losses that become more significant at higher frequencies. A SiC Schottky diode, by contrast, is a pure majority-carrier device: there is virtually no stored charge and therefore almost no reverse recovery current. This only becomes practical with SiC, because its high breakdown field strength allows Schottky contacts to sustain high blocking voltages with acceptable conduction losses – with silicon, Schottky diodes are only practical up to a few hundred volts.

Trench vs. Planar SiC MOSFET

In the planar SiC MOSFET, the channel lies horizontally at the wafer surface, similar to the Si DMOS. Trench SiC MOSFETs instead place the channel along the vertical wall of an etched trench. This avoids the JFET resistance of the planar structure (the constriction between two neighboring p-wells) and increases channel density – at the cost of more complex fabrication and higher demands on field shielding at the trench bottom, where locally elevated electric fields would otherwise threaten gate oxide reliability.

Trench vs. Planar SiC MOSFET

Two ways to form the channel



In the planar MOSFET, the p-well narrows current flow in the JFET region between the wells.
The trench MOSFET avoids this JFET resistance, but needs a field shield at the trench bottom.

The SiC/SiO2 Interface as a Challenge

Unlike with silicon, thermal oxidation of SiC leaves part of the carbon behind as interface defects. This elevated defect density at the SiC/SiO2 interface reduces the effective channel electron mobility to a fraction of the bulk value – a key reason why SiC MOSFETs long lagged behind their theoretical potential despite superior material properties. Process improvements such as NO or N2O post-oxidation annealing (nitrogen passivation) have significantly improved interface quality and therefore channel mobility in recent years.