Semiconductor Technology from A to Z

Advanced Packaging / 3D Integration

Limits of Classical Integration

Why “More Moore” Is Reaching Its Limits

For decades, the semiconductor industry followed Moore's law: the number of transistors per chip doubled roughly every 18–24 months, primarily through shrinking feature sizes. At feature sizes in the single-digit nanometer range, however, this scaling runs into physical and economic limits. Leakage currents rise due to short-channel effects, lithography cost per exposure step is exploding (EUV systems can cost well over 200 million euros), and yield drops disproportionately for large monolithic chips, since the probability of a defect grows with chip area.

At the same time, demand for computing power – driven not least by AI accelerators – calls for ever more transistors per system. The industry's answer increasingly lies not in smaller transistors but in a smarter arrangement and connection of multiple chips: advanced packaging.

“More than Moore” as an Alternative

Instead of integrating every function of a system onto a single monolithic die, individual functional blocks – processor cores, memory, I/O, analog circuitry – are implemented on separate chips, often manufactured in different technologies, and then tightly coupled into an overall system. This is known as heterogeneous integration. This strategy allows each building block to be manufactured in the technology best suited and most cost-effective for it (e.g. logic at 3 nm, memory in an older, cheaper node), instead of accepting compromises for a single manufacturing process.

The challenge thus shifts from the transistor to the interconnect technology between chips – from the question “how small can a transistor become?” to the question “how densely and how fast can two dies be connected to each other?”

Context: Classical Wire Bonding and Flip-Chip

The techniques covered in the assembly chapters – wire bonding and flip-chip – each connect a single die to a package or substrate. The electrical connections sit at the edge or on the chip surface and are limited in density: wire bonds typically achieve a pitch (spacing between adjacent connections) of 40–50 µm, while flip-chip bumps fall in the range of 100–150 µm.

Advanced packaging techniques such as TSV, interposers, and hybrid bonding

(covered in the following chapters) achieve interconnect densities that are orders of magnitude higher – down into the sub-micrometer range. Only this makes it possible to couple several dies so tightly that they behave electrically almost like a single monolithic chip.