Semiconductor Technology from A to Z

Advanced Packaging / 3D Integration

Through-Silicon Via (TSV)

The Principle

A through-silicon via is a vertical, electrically conductive connection that runs completely through the silicon substrate of a die. Unlike classical wiring layers, which sit exclusively on the chip surface, the TSV opens up the third dimension: signals and supply voltages can be routed from the front side of a die directly to the back side – and thus to the next die in a stack – without the detour via bond wires at the chip edge.

Fabrication Process

The process broadly breaks down into three approaches, which differ in when the via is created relative to the rest of the fabrication flow:

- Via-first: the TSV is etched into the bare wafer before transistor fabrication. This approach allows high-temperature-stable fill materials such as polycrystalline silicon, but is difficult to reconcile with modern CMOS processes.
- Via-middle: the TSV is created after transistor fabrication (FEOL) but before metallization (BEOL). This is the industrially dominant approach today, as it leaves the established transistor process untouched.
- Via-last: the TSV is etched only after the chip is fully fabricated, sometimes even from the wafer back side. The advantage is complete decoupling from front-side processing.

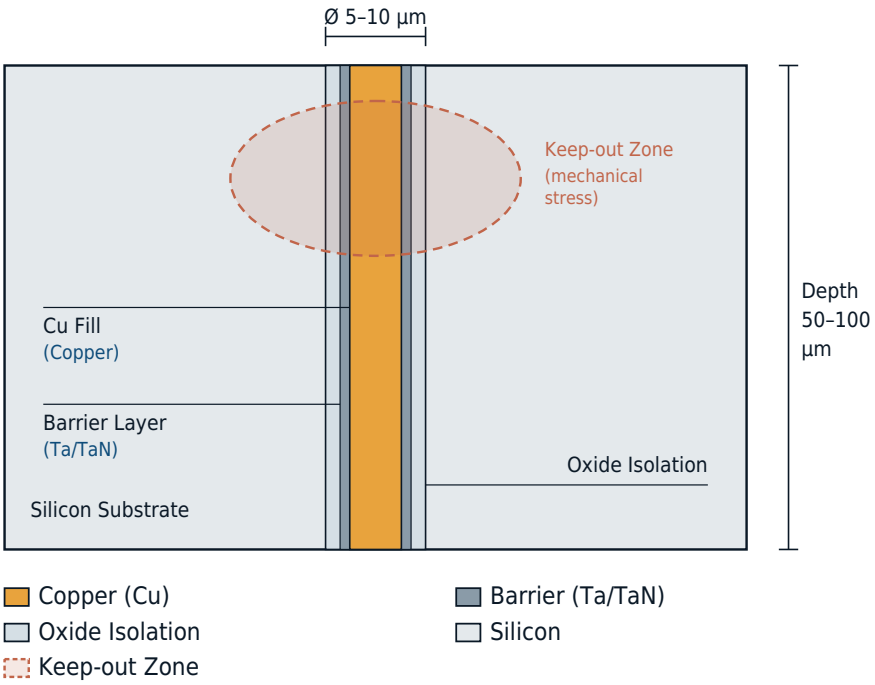
The via itself is etched using deep reactive ion etching (Bosch process, see the dry etching chapter) and reaches aspect ratios of 10:1 or higher – typical diameters are 5–10 µm, at depths of 50–100 µm.

Isolation and Cu Fill

Since the surrounding silicon is itself semiconducting, the via wall must first be electrically isolated with a thin oxide layer (usually via PECVD, see the deposition chapter). This is followed by a barrier layer (typically Ta/TaN) that prevents copper from diffusing into the silicon – the same issue encountered with copper metallization (see the copper technology chapter). Only after that is the via electrochemically filled with copper.

Structure of a TSV in cross-section

The Structure of a Through-Silicon Via (TSV)
Cross-section through a filled via in the silicon substrate



Challenges of the Aspect Ratio

The higher the aspect ratio, the more difficult it becomes to achieve complete, void-free copper filling – similar to the gap-fill problem in CVD processes, only on a much larger scale. In addition, because the thermal expansion coefficient of copper differs strongly from that of silicon, the filled-in copper creates mechanical stress in the surrounding material, which can degrade transistor performance in the immediate vicinity of the TSV (the “keep-out zone”).