Semiconductor Technology from A to Z

Advanced Packaging / 3D Integration

2.5D Integration: The Interposer

The Basic Principle

In 2.5D integration, several fully processed dies are not stacked directly on top of one another but placed side by side on a shared carrier substrate – the interposer. The interposer itself contains no active transistors; it serves purely as a high-density wiring layer that connects the individual dies to one another and to the package substrate beneath. The name “2.5D” reflects that an additional vertical layer is added, while the actual chip integration still happens laterally (side by side).

Silicon vs. Organic Interposer

- Silicon interposer: manufactured from a silicon wafer, penetrated by TSVs for through-connections and several metallization layers (RDL, see below) on top. Silicon allows very fine wiring structures (sub-micrometer pitch), but is comparatively expensive to produce and limited in area (typically to the size of a lithography reticle).
- Organic interposer: based on printed-circuit-board-like materials, significantly cheaper and producible in larger areas, but only achieves coarser wiring densities.

Redistribution Layer (RDL)

The redistribution layer is an additional metallization layer on the interposer (or directly on a die) that “redistributes” a chip's comparatively coarse contact pads onto the much finer connection structures of the interposer – hence the name. RDL structures are manufactured with lithography and copper technologies similar to the BEOL wiring of a regular chip, but with coarser feature widths and thicker traces, since current-carrying capacity matters more here than maximum density.

Example: HBM on an Interposer

The most prominent application example is the pairing of a logic die (e.g. a GPU) with several high-bandwidth-memory stacks on a shared silicon interposer. The extremely short, dense connection paths across the interposer enable memory bandwidths that classical PCB wiring could not achieve (covered in more depth in chapter 6).

Interposer with logic die and HBM stack

2.5D Integration: Interposer with Logic Die and HBM Stack
Cross-section of a shared silicon interposer