Semiconductor Technology from A to Z

Advanced Packaging / 3D Integration

Chiplets & Heterogeneous Integration

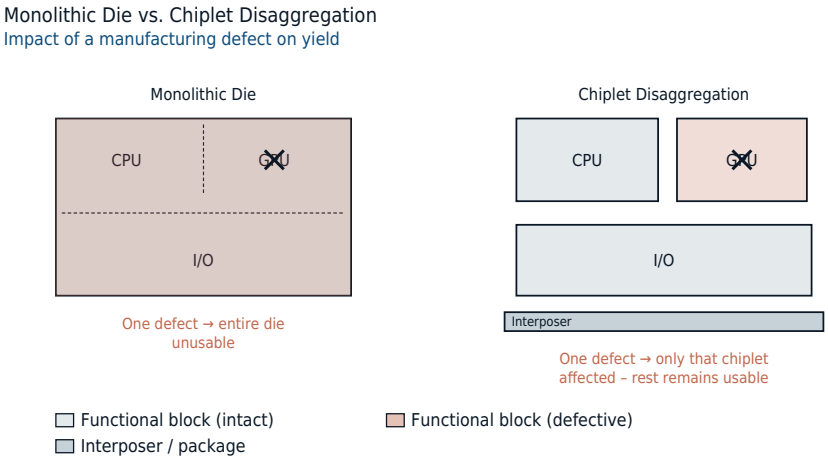
Disaggregation of SoCs

A classical system-on-chip (SoC) integrates every functional block – CPU cores, GPU, I/O controllers, memory interfaces – onto a single monolithic die. The chiplet approach deliberately breaks this SoC apart into several smaller, functionally distinct dies (“disaggregation”), which are then reassembled into a functionally coherent system using the advanced packaging techniques described in the previous chapters (interposer, hybrid bonding).

Advantages: Yield and Cost

The central advantage lies in manufacturing yield: since a chip's defect probability grows disproportionately with its area, the yield of one large monolithic die drops drastically faster than that of several smaller dies with the same total area. A defective small chiplet is discarded while the rest of the system can still be used – with a monolithic chip, the same defect causes total failure. In addition, as mentioned in chapter 1, each chiplet can be produced in whichever process node is economically and technically optimal for it, instead of committing the entire chip to the most expensive process it needs.

Impact of a defect: monolithic die vs. chiplet disaggregation



Disadvantages: Interconnect Overhead

These advantages come with a downside: the connection between chiplets – even via the densest advanced packaging techniques – has higher latency and higher energy consumption per transmitted bit than on-chip wiring within a monolithic die. System architects must therefore carefully weigh which functional blocks are coupled tightly enough to benefit from monolithic integration, and which are suited to being split into separate chiplets.

Standardization: UCIe

For chiplets from different manufacturers to be combined into a shared system, standardized physical and protocol-level interfaces are needed. The industry standard Universal Chiplet Interconnect Express (UCIe) defines both the electrical layer (signal levels, pitch, bump arrangement) and the transfer protocol, with the goal of enabling a vendor-independent “chiplet marketplace” analogous to today's standard IC procurement.