# Semiconductor Technology from A to Z

Advanced Packaging / 3D Integration

# Applications & Outlook

## HBM as a Flagship Example

High Bandwidth Memory is the most consistent commercial implementation of the technologies covered in this section: several DRAM dies (see the DRAM cell chapter) are connected via TSV and wafer-to-wafer or die-to-wafer bonding into a vertical stack of eight, twelve, or more layers, and then coupled to a logic die via a silicon interposer. The resulting memory bandwidth far exceeds that of classical DRAM modules wired planarly on a circuit board, while also achieving significantly lower energy consumption per transmitted bit.

## AI Accelerators

Modern AI training accelerators are the main driver behind the packaging technologies described here: they typically combine several logic chiplets with surrounding HBM stacks on a shared interposer, maximizing both the memory bandwidth critical to AI workloads and compute density, without depending on a single, uneconomically large monolithic die.

## Foundry Comparison

Different foundries have established their own brand names for their advanced packaging platforms, each combining and marketing the fundamental principles described in this section – interposer, TSV, hybrid bonding – in different ways. These platforms differ, among other things, in the choice of silicon versus organic interposer, the supported TSV aspect ratio, and the maximum number of dies that can be combined.

## Outlook

The trend clearly points toward ever tighter, ever more finely resolved 3D integration – from TSV-based stacks toward hybrid bonding with steadily shrinking pitch. At the same time, heat dissipation and cost remain the limiting factors, which is why advanced packaging today functions less as an outright replacement for classical transistor scaling and more as a necessary complement to it.