Semiconductor Technology from A to Z

Fundamentals

Bulk vs. SOI

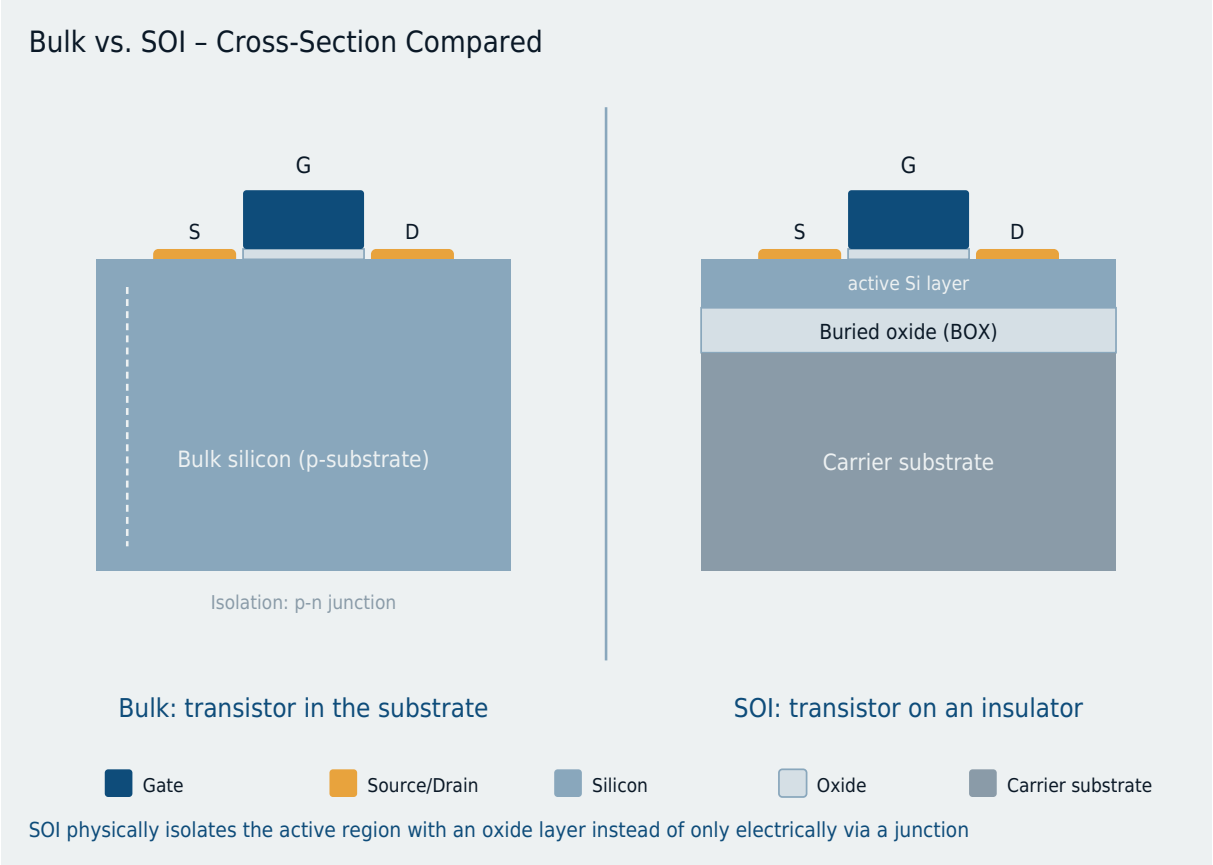
Overview

Bulk and SOI (Silicon-on-Insulator) are not different transistor types, but two different wafer technologies – the question is not *which* MOSFET is built, but *what it sits on*. Both approaches can be combined with the same basic principles from the MOSFET chapter; the difference lies solely in the substrate underneath and how the active region is electrically separated from it.

Structure Compared

In classic bulk technology, the transistor sits directly in a solid, homogeneous silicon wafer. Electrical separation from neighbouring devices and from the rest of the substrate is achieved through doped wells and the reverse-biased p-n junctions they form – an electrical, but not a physical, isolation.

SOI takes a different approach: beneath the thin, active silicon layer in which the transistors are fabricated lies a buried oxide layer (BOX) of silicon dioxide, with the actual carrier substrate only below that. This oxide layer physically and completely isolates the active region from the substrate – not just electrically via a junction, but through a genuine insulator.



Parasitic Effects and Isolation

This physical isolation has direct consequences: in bulk devices, a parasitic capacitance always exists between the active region and the substrate, impairing switching speed and power consumption. In addition, neighbouring n- and p-wells together with the substrate can form a parasitic thyristor structure that, under certain conditions, triggers (latch-up), rendering the circuit non-functional or even destroying it.

With SOI, the substrate capacitance is practically eliminated, since the buried oxide layer sits in between – enabling higher switching speeds at lower power dissipation. Latch-up is structurally impossible, since no continuous semiconductor path to the substrate exists. In addition, the thin, fully isolated active layer improves short-channel behaviour: the electric field from the drain can no longer spread as easily through the substrate to the channel, reducing unwanted short-channel effects such as DIBL – an advantage modern processes exploit for further scaling, similar to the FinFET.

Fabrication and Cost

Bulk wafers are a standard commodity: widely available, optimised for high yield

for decades, and comparatively cheap. SOI wafers, by contrast, require an additional manufacturing step just to create the buried oxide layer in the first place – usually via wafer bonding (two oxidised wafers are bonded together, and one is subsequently ground back to the desired thickness) or via SIMOX (oxygen ion implantation followed by annealing, which forms a buried oxide layer directly within the wafer). Both methods make SOI wafers considerably more expensive than bulk material.

A further distinction is made between PD-SOI (Partially Depleted) and FD-SOI (Fully Depleted): with PD-SOI, the active silicon layer is thick enough that a neutral, "floating" region remains in the channel – similar to bulk, but with reduced substrate capacitance. With FD-SOI, the layer is thin enough that it becomes fully depleted under operating voltage (no neutral region remains), which further improves short-channel behaviour and is used today mainly in energy-efficient and mixed-signal applications.

Comparison Table

Property	Bulk	SOI
Isolation from substrate	electrical (p-n junction)	physical (oxide layer, BOX)
Parasitic capacitance	present	strongly reduced
Latch-up risk	present	structurally excluded
Short-channel behaviour	standard	improved
Cost	low	considerably higher
Typical application	mass-market logic	high-performance/low-power/RF applications