

Semiconductor Technology from A to Z

Analog & Mixed-Signal Design

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ADC Architectures

Fundamentals: Sampling, Quantization, Resolution

An analog-to-digital converter (ADC) converts a continuous-time, continuous-amplitude signal into a sequence of discrete numerical values. This process consists of two separate steps: sampling in time and quantization of the amplitude.

According to the Nyquist-Shannon sampling theorem, the sampling frequency must be at least twice the highest frequency component contained in the signal in order to reconstruct it without loss of information. Otherwise, aliasing produces indistinguishable mirror frequencies – in practice, an analog anti-aliasing filter therefore usually precedes the ADC.

Quantization rounds the sampled voltage to the nearest of 2^N representable codes (for N-bit resolution). The resulting unavoidable difference is the quantization error, which appears as quantization noise in the output signal. Key parameters for evaluating real converters are SNR (signal-to-noise ratio), SFDR (spurious-free dynamic range), and ENOB (effective number of bits) – the actually usable resolution accounting for noise and distortion.

SAR ADC (Successive Approximation Register)

The SAR ADC converts a sampled voltage into a digital code through a binary search. An internal register tests bit by bit, starting with the most significant bit (MSB), whether the corresponding code value lies above or below the input voltage, using an internal DAC to generate the comparison voltage and a comparator to make the decision.

For a resolution of N bits, the conversion requires exactly N comparison cycles – conversion speed therefore scales linearly with resolution. SAR ADCs feature small area, low power consumption, and moderate-to-high resolution (typically 8–18 bits) at medium sample rates (kHz to a few tens of MHz), making them today's most widely used ADC architecture in mixed-signal ICs.

Pipeline ADC

The pipeline ADC splits the conversion across several stages connected in series. Each stage converts a few bits with a simple flash sub-ADC, reconstructs a reference signal from these bits via an internal DAC, forms the difference from the input signal (the residue), and amplifies this residue for the next stage

(multiplying DAC, MDAC).

Because all stages work simultaneously on different samples (pipelining), this architecture achieves significantly higher throughput than a SAR ADC at comparable resolution – typically 8-16 bits at sample rates from tens of MHz to the GHz range. Drawbacks are the latency introduced by the pipeline stages and higher area and power requirements compared to a SAR ADC.

Sigma-Delta ADC

The sigma-delta ADC (also delta-sigma ADC) takes a fundamentally different approach: instead of high per-sample amplitude resolution, it uses strong oversampling (typically 32-256× the Nyquist rate) combined with a feedback sigma-delta modulator. At its core, this consists of an integrator, a coarse (often 1-bit) quantizer, and feedback through a DAC into the signal path.

The feedback pushes quantization noise to higher frequencies (noise shaping), which is then removed by a digital low-pass (decimation) filter that simultaneously reduces the high sample rate back to the actual Nyquist rate. Sigma-delta ADCs thereby achieve very high effective resolutions (beyond 24 bits) at low-to-moderate bandwidths and are standard in precision instrumentation, audio, and sensing.

Flash ADC

The flash ADC is the fastest but also the most resource-intensive ADC architecture: the input voltage is compared in parallel against $2^N - 1$ reference voltages derived from the reference via a resistor ladder. A downstream priority encoder converts the resulting thermometer-coded comparator pattern into a binary code.

Because conversion happens within a single clock cycle, the flash ADC achieves the highest available sample rates (several GHz). However, the comparator count – and thus the required area and power – grows exponentially with resolution, limiting practical resolution to typically 6-8 bits. Flash ADCs are therefore used mainly in high-speed applications, often as a fast sub-ADC stage within a pipeline ADC.

Comparison & Application Areas

Architecture	Typ. resolution	Typ. sample rate	Typical application
SAR	8-18 bit	kHz – approx. 50 MHz	General purpose, sensing, mixed-signal SoCs

Architecture	Typ. resolution	Typ. sample rate	Typical application
Pipeline	8-16 bit	10 MHz - GHz	Communications, video, RF receivers
Sigma-Delta	up to >24 bit	Hz - a few MHz	Precision instrumentation, audio, sensing
Flash	6-8 bit	>1 GHz	High-speed digitization, oscilloscopes

Choosing an architecture is always a trade-off between resolution, speed, area, and power consumption. Modern SoCs also combine architectures depending on the application, such as pipeline stages with flash sub-ADCs, or SAR stages within time-interleaved ADC architectures for the highest sample rates at moderate resolution.