Semiconductor Technology from A to Z

Analog & Mixed-Signal Design

DAC Architectures

Fundamentals: Resolution, INL/DNL, Settling Time

A digital-to-analog converter (DAC) generates an analog voltage or current from an N-bit digital code, selecting from 2^N possible discrete output values.

Two parameters are used to evaluate linearity: DNL (Differential Non-Linearity) describes the deviation of the spacing between two adjacent output codes from the ideal LSB step – a DNL ≤ –1 LSB results in non-monotonic behavior. INL (Integral Non-Linearity) describes the cumulative deviation of the entire transfer curve from the ideal straight line.

For dynamic evaluation, the settling time is decisive: the time required for the output to settle within a defined error band (e.g. ±½ LSB) after a code change. It limits the maximum update rate of the DAC and is influenced by the bandwidth of the output stage (often an op-amp buffer).

R-2R DAC

The R-2R DAC uses a resistor network built from only two resistor values (R and 2R), which can be cascaded to any number of bits without – unlike a binary-weighted resistor network – requiring extreme resistance ratios between the MSB and LSB. At each node of the network, a switch connects either to ground or to the reference voltage depending on the bit value.

The major advantage is good manufacturability using just two precisely matched resistor values, which reduces area and matching requirements. Achievable accuracy, however, depends strongly on the matching of the switch transistors and resistors; R-2R DACs are commonly used for resolutions in the 8–16 bit range at moderate speeds.

Current-Steering DAC

The current-steering DAC is the dominant architecture for high speed. It consists of an array of binary- or thermometer-weighted current sources that are steered, depending on the digital code, into one of two output branches (differential). An output resistor or transimpedance stage converts the resulting output current into a voltage.

Since no internal op-amps with limited bandwidth sit in the signal path, current-steering DACs achieve very high sample rates (up to the GHz range) at typical resolutions of 8–16 bits. The most significant bits are usually implemented with

thermometer-coded segmentation to guarantee monotonicity and minimize glitches at code transitions, while the least significant bits are realized as binary-weighted (segmented architecture).

Sigma-Delta DAC

Analogous to the sigma-delta ADC, the sigma-delta DAC uses oversampling and noise shaping, but in the reverse signal direction: a digital interpolation filter first raises the data rate of the input signal, a digital sigma-delta modulator then reduces the word width (often to 1 bit) while pushing the quantization noise to high frequencies. A very simple, highly linear 1-bit DAC converts the resulting bitstream, and an analog low-pass filter smooths the result into the final analog signal.

Since the actual DAC core resolves only 1 bit, the matching problem of multi-bit resistor or current-source arrays is almost entirely eliminated – at the cost of a higher required clock rate and digital filter complexity. Sigma-delta DACs therefore dominate high-resolution audio applications (typically 16–24 bits).

Comparison & Application Areas

Architecture	Typ. resolution	Typ. speed	Typical application
R-2R	8–16 bit	low – moderate	General signal generation, control systems
Current-Steering	8–16 bit	up to GHz range	RF transmit chains, direct digital synthesis
Sigma-Delta	16–24 bit	low – moderate (audio bandwidth)	Audio DACs, precision signal generation

As with ADCs, the application determines the architecture: high speed at moderate resolution favors current-steering, high resolution at moderate bandwidth favors sigma-delta. R-2R DACs are found today mainly where simple, robust signal generation is sufficient without high-speed requirements.