Semiconductor Technology from A to Z

Devices

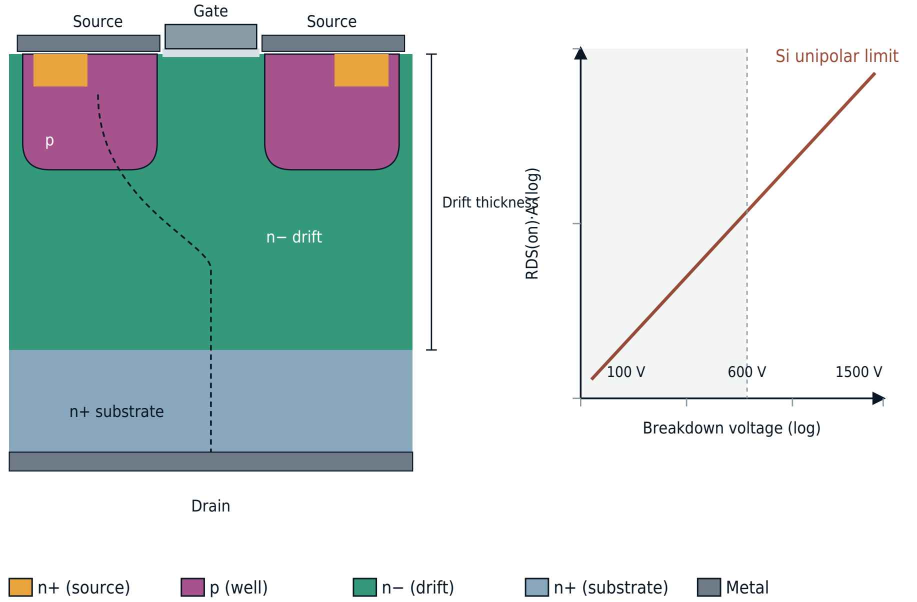
Si Power Devices (Power MOSFET, IGBT)

The Si Power MOSFET: Structure and the $R_{DS(on)}$ Dilemma

The vertical Si power MOSFET (usually built as a DMOS – Double-Diffused MOS – device) carries current vertically through the wafer: source and gate sit on the top surface, the drain contact on the wafer backside. This geometry allows high currents in a compact chip area, since the entire chip area serves as the current cross-section. The decisive drawback appears as blocking voltage rises: on-resistance $R_{DS(on)}$ grows roughly with the 2.5th power of the breakdown voltage, because silicon’s low critical field strength requires a thick, lightly doped drift layer to absorb the electric field while blocking. This relationship is exactly what underlies the Baliga figure of merit introduced in the compound-semiconductor chapter as a power-device benchmark – and explains why classic Si MOSFETs quickly become uneconomical above a few hundred volts.

Vertical Si Power MOSFET (DMOS)

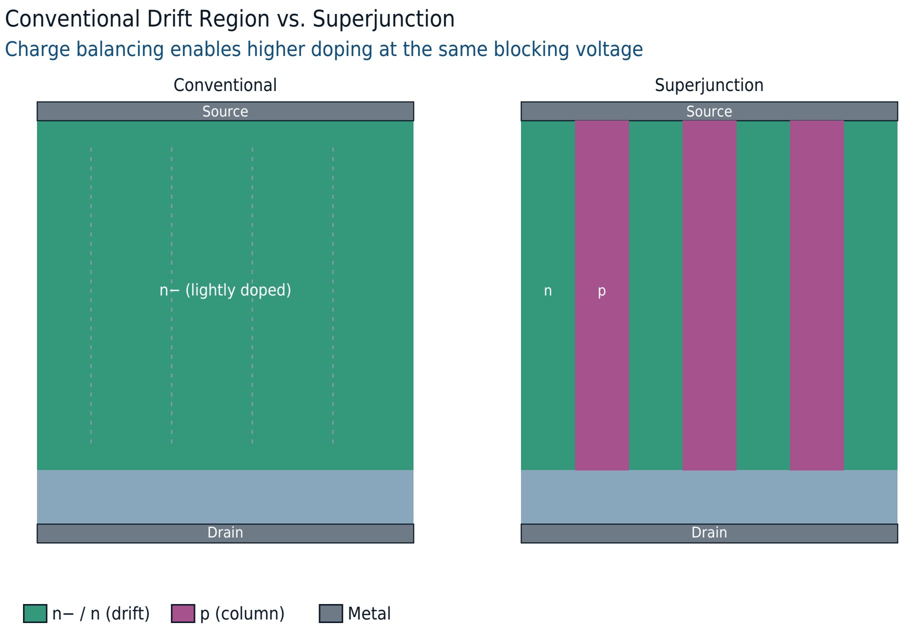
Structure and the RDS(on) breakdown-voltage tradeoff



Silicon's low critical field strength requires a thick, lightly doped drift layer – on-resistance therefore grows disproportionately with voltage.

Superjunction MOSFETs: Breaking the Classic Tradeoff

Starting in the mid-1990s, superjunction technology (known under brand names such as CoolMOS) partially broke this relationship. Instead of a uniformly lightly doped drift region, narrow p- and n-columns are alternately introduced that mutually deplete each other laterally when blocking (“charge balancing”). This allows the n-drift region to be doped considerably more heavily without reducing breakdown voltage – $R_{DS(on)}$ then scales only roughly linearly with voltage instead of by a high power. Superjunction MOSFETs today dominate the roughly 500 to 900 V range (switched-mode power supplies, PFC stages) and are therefore silicon’s strongest competitor to GaN HEMTs in this voltage window – though with lower switching frequency due to higher output capacitance.

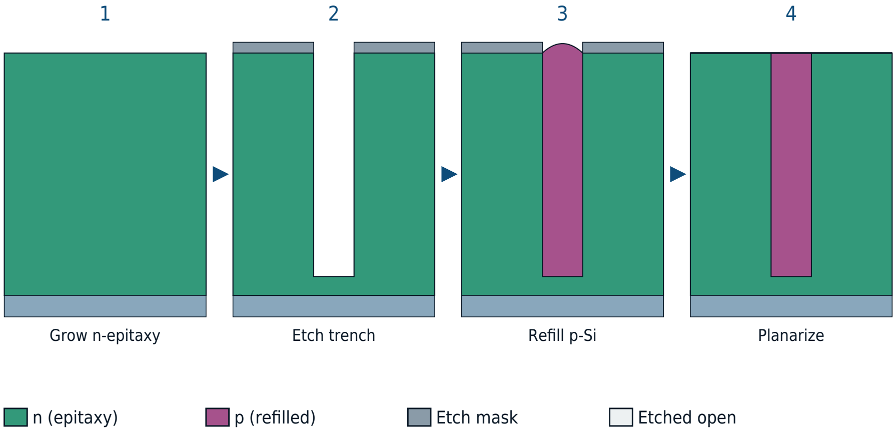


Alternating p-/n-columns mutually deplete each other laterally when blocking – the n-columns can therefore be doped more heavily without lowering breakdown voltage.

The gate itself is unaffected: as in a classic power MOSFET, it sits at the very top surface and controls the channel in the uppermost p-well, which is electrically connected to the p-columns beneath it. The columns themselves carry no channel – they exist solely to shape the field in the drift region. Because the columns are 40 to 60 µm deep, ordinary diffusion or implantation cannot produce them. The trench-fill process has become the standard approach: a deep, narrow trench is dry-etched into the finished n-epitaxial layer (deep reactive ion etching) and then epitaxially refilled with p-doped silicon, followed by CMP planarization of the surface. Older process generations instead used multi-epitaxy: several thin epitaxial steps each with local p-implantation, which only merge into a continuous column during a final high-temperature diffusion – more process steps, but without the demanding trench etch.

Superjunction Fabrication: Trench-Fill Process

Deep p-columns are formed by trench etching and epitaxial refill



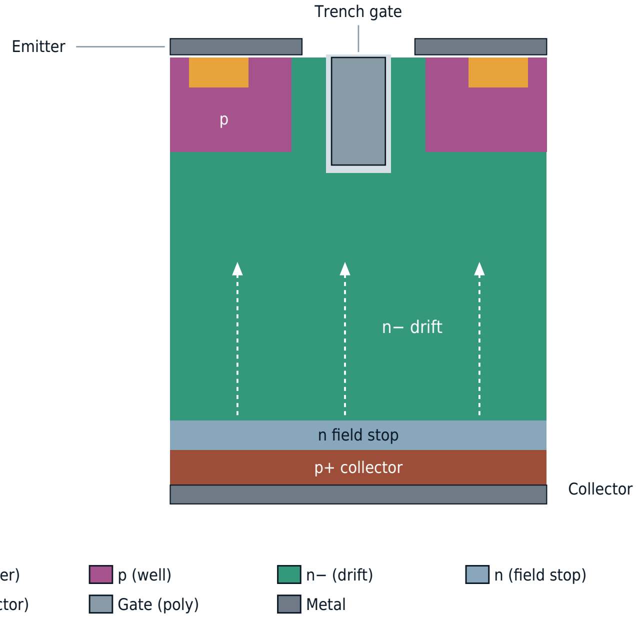
A deep, narrow trench is dry-etched and then epitaxially refilled with p-doped silicon – CMP planarizes the surface as the final step.

The IGBT: Bipolar Amplification for High Voltages

For the high-voltage range above roughly 600 V, where even the superjunction MOSFET reaches its limits, the IGBT (Insulated Gate Bipolar Transistor) combines a MOSFET gate with a bipolar pnp output stage. The additional carrier injection from the p+ collector layer floods the drift region with minority carriers (conductivity modulation), drastically lowering on-resistance – far below what a purely unipolar MOSFET could achieve at the same blocking voltage. The price is delayed turn-off behavior: the so-called tail current arises because the carriers stored in the bulk cannot be switched off via the gate field as in a MOSFET, but must instead be removed through slower recombination and sweep-out. This costs switching-loss power and limits practical switching frequency to typically a few tens of kHz.

Trench Field-Stop IGBT Cross-Section

A MOSFET gate controls a bipolar pnp output stage



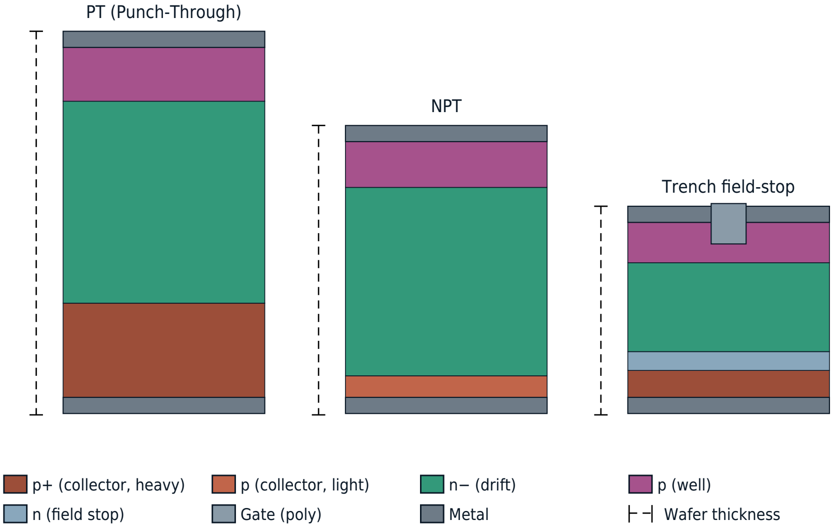
The p+ layer injects holes into the drift region (conductivity modulation) – the field-stop layer allows a thinner drift region at the same blocking voltage.

IGBT Generations: From Planar PT to Trench Field-Stop

IGBT development over the last three decades can be read as a continuous reduction in drift-layer thickness alongside improved short-circuit ruggedness. Early planar PT (punch-through) IGBTs used thick epitaxial layers on a heavily doped p+ substrate. Second-generation NPT (non-punch-through) IGBTs dispensed with epitaxy in favor of thinner, homogeneously doped wafers with a lightly doped collector – improving short-circuit ruggedness at the cost of somewhat higher conduction losses. Today’s dominant trench field-stop generation combines a vertical trench gate structure (instead of a planar gate, for higher channel density and lower channel resistance) with a thin n field-stop layer near the backside. This field-stop layer absorbs the electric field similarly to the PT concept, but permits considerably thinner wafers than the original PT generation – simultaneously reducing both conduction and switching losses, goals long considered mutually exclusive.

IGBT Generations Compared

Decreasing wafer thickness with increasing short-circuit ruggedness



From thick epitaxy on a p+ substrate (PT) through homogeneously doped NPT wafers to the thin trench field-stop IGBT – each generation cuts conduction and switching losses.

Silicon in System Comparison: Where the Established Technology Still Dominates

Despite the technical superiority of SiC and GaN in switching frequency and specific power loss, silicon remains the most cost-effective choice wherever voltage and switching frequency are moderate: industrial drives, uninterruptible power supplies, household appliances, and much of rail and grid applications continue to rely on IGBTs. What matters is decades of manufacturing maturity, large wafer diameters up to 300 mm, and established, low-cost packaging technology (e.g. wire bonding instead of the more elaborate interconnect technology that SiC/GaN modules often require due to higher switching speeds). Switching to SiC/GaN pays off economically above all where higher switching frequencies enable smaller magnetics and lower cooling costs, offsetting the higher component price over the system’s lifetime – a criterion already described as a cost trend in the SiC/GaN/Si system-comparison chapter.