Semiconductor Technology from A to Z

Devices

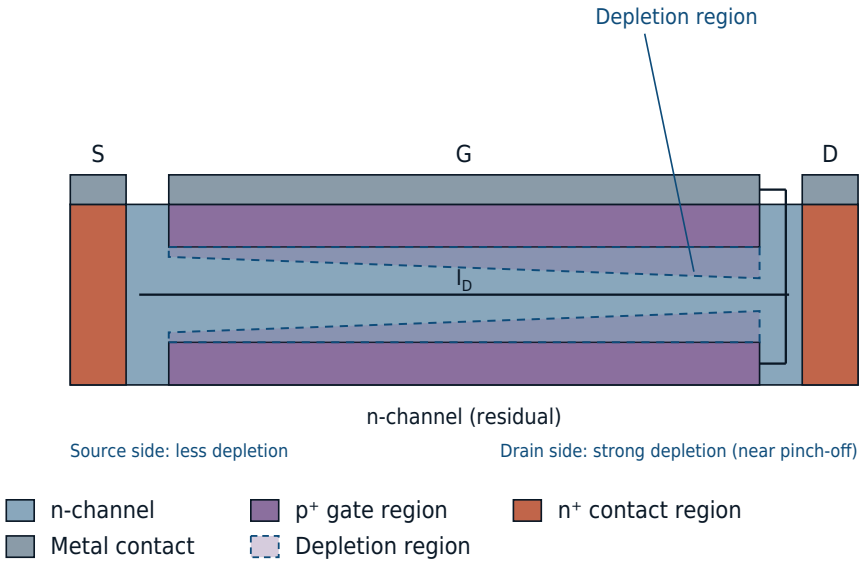
The Junction FET (JFET)

Structure

An n-channel JFET consists of a continuous channel of n-doped semiconductor material, usually silicon. On opposite sides of the channel (in a planar layout) or surrounding it (in a symmetric layout), heavily p^+-doped regions are introduced, which together form the gate terminal. Ohmic source and drain contacts are located at the two ends of the channel. Because the channel is physically symmetric between source and drain, the two terminals are in principle interchangeable for most JFETs – it is the external circuit that determines which terminal serves as the source (reference potential). In p-channel JFETs, the doping types and polarities are reversed accordingly.

Structure and Depletion Region of an n-Channel JFET

Planar layout with two p^+ gate regions



V_{GS}
from the p^+ regions into the channel and pinches it off. Because
V_{DS}
more pronounced at the drain end than at the source end
(wedge-shaped depletion region).

Operation: Depletion Region and Pinch-off

The pn junction between gate and channel is always reverse-biased during operation (for an n-channel JFET, $V_{GS} \leq 0\,\mathrm{V}$). This creates a depletion region that

is essentially free of mobile charge carriers and therefore does not contribute to current flow. As the reverse bias increases, this region grows into the channel and narrows its conductive cross-section. Because the drain-source voltage V_{DS} itself produces a voltage drop along the channel, the depletion region is more pronounced at the drain end than at the source end – the channel therefore narrows in a wedge shape. Once the depletion region reaches the opposite edge at a sufficiently high voltage, the channel is completely pinched off.

Output Characteristics

The output characteristic curves (I_D vs. V_{DS} for various V_{GS}) show three distinct regions: In the ohmic (linear) region (small V_{DS}), the JFET behaves approximately like a voltage-controlled resistor whose resistance depends on V_{GS}. In the pinch-off or saturation region ($V_{DS} > V_{DS,sat}$), I_D remains nearly constant, since the channel is already pinched off at the drain end and further increases in voltage have little additional effect on current. The drain current in saturation can be approximated by the Shockley equation:

$$I_D = I_{DSS} \cdot (1 - V_{GS} / V_p)^2$$

Here I_{DSS} is the maximum drain current at $V_{GS} = 0\,V$, and V_p is the pinch-off voltage. In the breakdown region (very large V_{DS}), avalanche breakdown eventually occurs at the drain-side pn junction, which can destroy the device.

Small-Signal Behavior

For use as an amplifying element, the transconductance $g_m = \partial I_D / \partial V_{GS}$ is the key parameter, indicating how strongly the drain current changes for a small change in gate-source voltage. Because the JFET is voltage-controlled with very low gate current, it offers an extremely high input impedance, making it – much like the MOSFET – well suited to high-impedance signal sources.

Properties and Applications

Because the gate is always reverse-biased, gate leakage current is extremely low, making JFETs a preferred choice for low-noise input stages, such as in operational amplifiers, electrometer amplifiers, and high-quality audio equipment. Other classic applications include voltage-controlled resistors (chopper circuits), simple constant-current sources (by shorting gate to source), and RF switches. Since JFETs have no sensitive oxide layer, they are more robust against electrostatic discharge (ESD) than MOSFETs. On the downside, JFETs cannot be operated in enhancement mode, and because of the lateral extent of the gate regions they scale less well than MOSFETs – which is why

they play no role in highly integrated digital circuits.