Semiconductor Technology from A to Z

Reliability

Electromigration, TDDB and NBTI/PBTI

Electromigration

Electromigration refers to the transport of material within a metal conductor caused by the momentum transfer from drifting conduction electrons to the metal ions of the crystal lattice, often called the electron wind. At the high current densities of modern interconnect levels, on the order of several MA/cm², metal atoms preferentially migrate along grain boundaries in the direction of current flow. Material accumulates on the anode side, forming hillocks, while vacancies coalesce into voids on the cathode side, which can narrow the conductor cross-section until it fails completely.

The mean time to failure of an interconnect due to electromigration is described by the empirical Black equation $MTTF = A \cdot J^{-n} \cdot e^{E_a/(k \cdot T)}$, where J is the current density, T the temperature, E_a the activation energy, k the Boltzmann constant, and the current density exponent n is typically close to 2. For aluminum interconnect, the allowable design current density is usually in the range of 1 to 2 MA/cm² with an activation energy of about 0.5 to 0.7 eV along grain boundaries; copper, with an activation energy of roughly 0.7 to 1.1 eV and lower self-diffusion, achieves a much higher electromigration resistance at the same current density. This improvement was one of the key drivers behind the introduction of copper interconnect technology in the 1990s, since it was what first made higher current densities reliably possible as wire cross-sections continued to shrink.

Time-Dependent Dielectric Breakdown (TDDB)

Time-dependent dielectric breakdown (TDDB) describes the delayed electrical breakdown of a gate dielectric under continuous stress well below its intrinsic breakdown voltage. The cause is the continuous generation of defects in the oxide by injected charge carriers, which over time link up into a continuous low-resistance path between gate and channel, as described by the percolation model.

In modern CMOS technologies, the effective gate oxide thickness (equivalent oxide thickness, EOT) is only about 1 to 2 nm, which already produces electric field strengths of 8 to 12 MV/cm in the oxide during normal operation – a regime in which TDDB becomes the dominant lifetime-limiting mechanism. Because the defect density required to trigger breakdown also decreases with oxide thickness, TDDB is one of the central reasons why the maximum allowable operating voltage of modern technologies cannot simply be increased. In

qualification testing, lifetime is typically determined through accelerated tests at field strengths of 15 MV/cm and above combined with elevated temperature, and extrapolated to nominal operating conditions using a power law, with required lifetimes of ten years having to be achieved at fields well below the test conditions.

Bias Temperature Instability (NBTI/PBTI)

Bias temperature instability (BTI) refers to the time-dependent shift of a MOS transistor threshold voltage under sustained gate bias at elevated temperature. In PMOS transistors, the effect appears as negative BTI (NBTI) under negative gate-source voltage, while in NMOS transistors it appears as positive BTI (PBTI) under positive gate-source voltage; both manifest as an increase in the magnitude of the threshold voltage and a corresponding reduction in drain current over the operating lifetime.

The generation of interface states at the Si–SiO_2 interface and the trapping of charge carriers within the gate dielectric are considered the main causes, and part of the shift recovers once the gate bias is removed. Typical threshold voltage shifts after ten years of operation are on the order of 30 to 80 mV, depending on technology, operating temperature, and supply voltage; in high-k metal-gate technologies, NBTI usually dominates over PBTI. Because BTI continuously reduces the switching speed of logic paths over the lifetime of a chip, the effect is accounted for during timing signoff through an aging guardband, often several percent, applied to the threshold voltage or gate delay.