Semiconductor Technology from A to Z

Digital technology

Static Timing Analysis: Setup and Hold Time

Fundamentals of Static Timing Analysis

Static timing analysis (STA) checks whether a digital circuit operates reliably at a given clock frequency without actually running the circuit as in a simulation. To do this, every path between two consecutive flip-flops is examined: the launching flip-flop produces its value at the output after the clock-to-Q delay t_{CQ} – typically in the range of 20 to 100 picoseconds depending on technology and cell –, the value then propagates through the combinational logic with delay t_{logic}, and must arrive at the data input of the capturing flip-flop before it can be latched.

For the capturing flip-flop to sample the value correctly, the signal must already be stable for a certain time before the active clock edge (setup time t_{setup}, often 20 to 50 ps) and must not change for a certain minimum time after the clock edge either (hold time t_{hold}, often just a few picoseconds up to about 20 ps). If these timing windows are violated, the flip-flop can enter a metastable state in which the output oscillates between the two logic levels for an indefinite time.

The Setup Check

The setup check ensures that a signal arrives at the destination register in time before the next clock edge. For a clock period T with clock skew Δt_{skew} between the launching and capturing flip-flop, the condition is $T + \Delta t_{skew} \geq t_{CQ} + t_{logic} + t_{setup}$. The difference between the available time and the time actually required is called the setup slack; if the slack is negative, the path violates the required clock frequency and must be fixed using faster cells, fewer logic stages, or a reduced clock frequency. For example, with a clock period of 1 ns (corresponding to 1 GHz), a t_{CQ} of 40 ps, a logic delay of 700 ps, and a setup time of 30 ps, the resulting slack is about 230 ps – clearly positive and therefore not critical.

The critical path of a circuit is the path with the smallest setup slack; it determines the maximum possible clock frequency of the entire chip. Because manufacturing variation, supply voltage, and temperature all affect gate delays, which can vary by 20 to 30 %, the setup check is always performed for the slowest specified process, voltage, and temperature condition (the slow corner).

The Hold Check and the Role of Clock Skew

The hold check ensures that a signal does not arrive at the destination register

too quickly and overwrite the value still needed from the previous clock period before the new clock edge has reached the destination register. The condition is $t_{CQ} + t_{logic} \geq t_{hold} + \Delta t_{skew}$; unlike the setup check, the clock period T plays no role here, since hold violations occur independently of the clock frequency and therefore cannot be fixed by clocking the circuit more slowly.

Hold violations are instead corrected by deliberately inserting additional buffer cells into the affected path, which artificially increase the signal delay t_{logic} – a single buffer stage typically adds 10 to 30 ps of extra delay, depending on cell size and technology. Because the hold check is most critical at the fastest specified process, voltage, and temperature condition (the fast corner), static timing analysis is typically carried out across several such corner cases – often a combination of at least slow-slow, typical-typical, and fast-fast conditions at multiple voltage and temperature points – to rule out both setup and hold violations under all operating conditions.