Semiconductor Technology from A to Z

Analog & Mixed-Signal Design

PLL – Phase-Locked Loop

Basic Principle of the Feedback Loop

A phase-locked loop (PLL) is a feedback system that aligns the phase and frequency of an internal oscillator to a reference signal. The three core blocks are a phase detector, which measures the phase difference between the reference and feedback signals, a loop filter, which smooths this error signal, and a voltage-controlled oscillator (VCO), whose output frequency is proportional to the applied control voltage and which typically has a tuning range of 20 to 50 % of its center frequency.

In the locked state, the phase of the VCO output follows the reference phase with a constant, ideally vanishing residual error. If the reference frequency changes or the VCO drifts, the feedback loop adjusts the VCO control voltage until the phase error is minimized again; the required lock time typically ranges from a few microseconds to several hundred microseconds, depending on the loop bandwidth.

Phase-Frequency Detector, Charge Pump, and Frequency Divider

In digital PLLs, the phase difference is usually determined with a phase-frequency detector (PFD), which, in addition to the pure phase deviation, also determines which of the two signals is leading and uses this to drive a charge pump with typical currents from a few tens of microamperes up to a few milliamperes. The charge pump charges or discharges a capacitor in the loop filter proportionally to the detected phase difference, generating the control voltage for the VCO.

If a programmable frequency divider with division ratio N is inserted between the VCO output and the feedback input, the loop locks to an output frequency $f_{out} = N \cdot f_{ref}$. A typical example from mobile communications is generating a carrier frequency of about 2.4 GHz from a stable 26 MHz crystal oscillator with a division ratio N of around 92 – this principle of frequency synthesis allows a wide range of different but equally stable output frequencies to be generated from a single, highly stable reference frequency.

Loop Bandwidth, Jitter, and Applications

The bandwidth of the loop filter involves an important trade-off: a wide loop bandwidth effectively suppresses the VCO phase noise but passes through the noise of the reference and the phase detector almost unfiltered; a narrow

bandwidth, conversely, filters out reference noise but can no longer suppress the intrinsic VCO phase noise at larger offsets from the carrier. In practice, the loop bandwidth is often set to about one-tenth to one-twentieth of the reference frequency to balance both noise contributions; typical integrated PLLs for clocking applications achieve total RMS jitter in the range of a few picoseconds to a few tens of picoseconds.

PLLs are used, among other things, for clock generation and clock multiplication in digital circuits, for frequency synthesis in radio transmitters and receivers, and for clock and data recovery from serial data streams at rates of several gigabits per second, where the PLL reconstructs the embedded clock of a received signal without a separate clock line.