

Semiconductor Technology from A to Z

Digital technology

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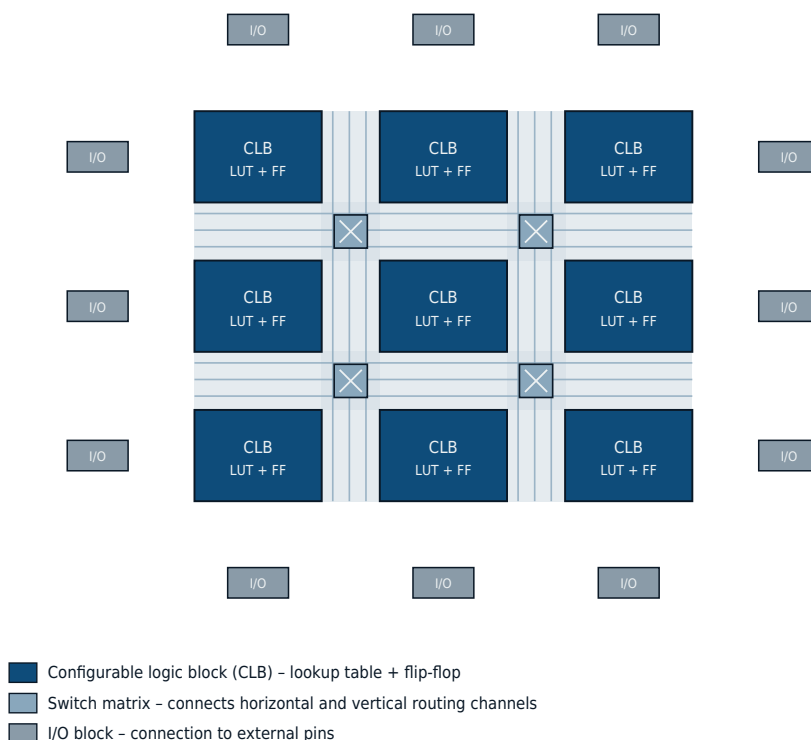
FPGA vs. ASIC: Synthesis Flow and HDL

Two Paths from Circuit Design to Silicon

There are fundamentally two paths for turning a digital circuit design into hardware. An ASIC (Application-Specific Integrated Circuit) is designed for exactly one application and manufactured as a standard-cell layout using the process steps described in earlier chapters – photolithography, etching, doping, metallization; its function is fixed and unchangeable after fabrication. An FPGA (Field-Programmable Gate Array), by contrast, consists of a grid of prefabricated but configurable logic blocks (typically lookup tables with a few inputs, combined with flip-flops) and a programmable interconnect network, whose function is only determined after manufacturing – and can be reprogrammed arbitrarily often in the field – via a configuration bitstream.

Basic FPGA Architecture

Configurable logic blocks and programmable interconnect network



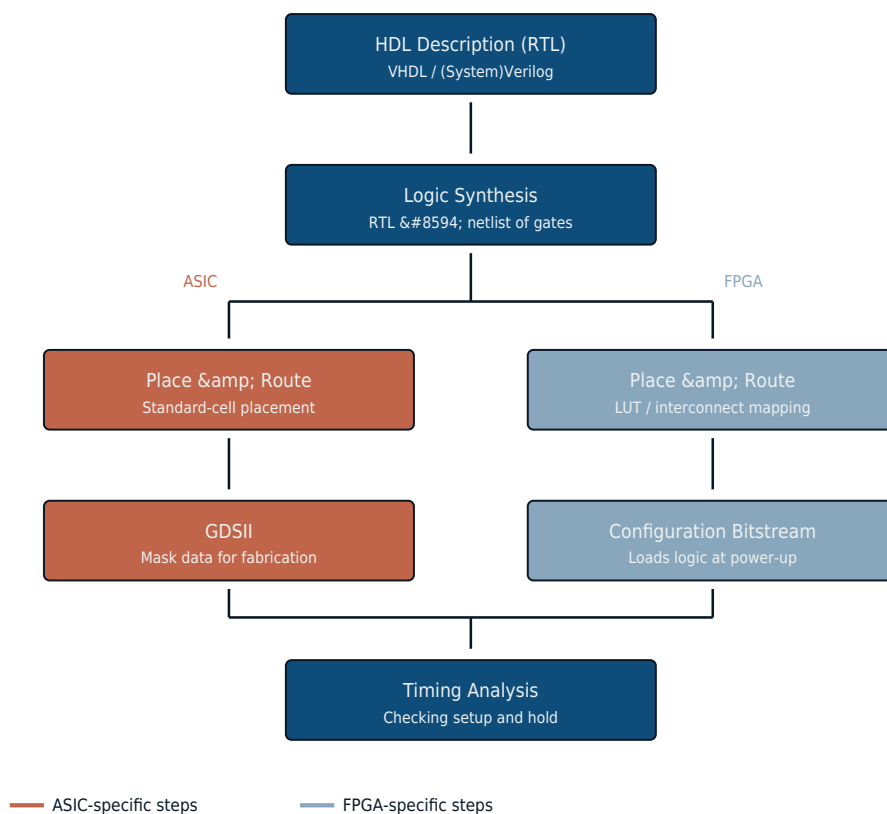
The fundamental difference therefore lies in when the function is fixed: in an ASIC, the wiring is physically cast into metal layers, while in an FPGA it is emulated electronically – with corresponding trade-offs in area, speed, and power consumption.

Hardware Description Languages and the Synthesis Flow

Both ASICs and FPGAs today are designed almost exclusively using hardware description languages (HDLs) such as VHDL or (System)Verilog, which describe the desired circuit behavior at the register-transfer level (RTL) – that is, as a data flow between registers and the combinational logic in between, without yet fixing concrete gates. A logic synthesis tool automatically translates this RTL description into a netlist of actual gates (for an ASIC, from a standard-cell library; for an FPGA, from lookup tables and flip-flops), optimizing according to given targets for area, speed, and power.

Synthesis Flow: From HDL to Silicon

Shared steps, then separate paths for ASIC and FPGA



Afterward, for an ASIC, the place-and-route step handles the physical placement of cells and wiring on the chip before the mask data (GDSII) for fabrication is generated; for an FPGA, a comparable step maps the logic onto specific lookup tables and interconnect resources of the target chip before a configuration bitstream is generated, which is loaded into the FPGA at power-up. Both flows conclude with a timing analysis that ensures all paths meet the setup and hold

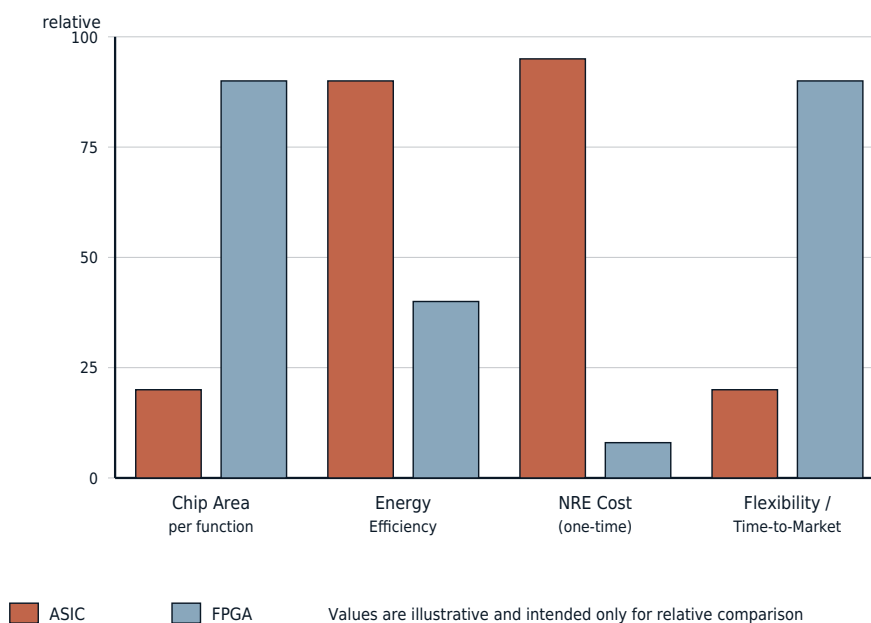
conditions described in the previous chapter at the target frequency.

When FPGA, When ASIC?

FPGAs are particularly suited to prototyping, small to medium production volumes, and applications that still need to be adapted after deployment, since their function can be reprogrammed at any time without requiring new masks or a new fabrication run. This flexibility comes at a cost, however: FPGAs typically require several times the chip area of a comparable ASIC for the same function, run at lower clock speeds, and consume markedly more energy per operation, since a significant portion of the chip area is reserved for programmable interconnect and configuration memory rather than actual logic.

FPGA vs. ASIC Comparison

Illustrative relative comparison across four criteria



ASICs, by contrast, achieve the best possible area, speed, and energy efficiency for a fixed function, but require high one-time development costs (non-recurring engineering, NRE) for the mask set and verification, which only pay off at correspondingly high production volumes – especially in advanced technology nodes, where mask costs can run into the tens of millions – as well as significantly longer development times to production readiness. As a middle ground, some vendors offer structured-ASIC approaches or embedded FPGA blocks (eFPGA) within an ASIC, retaining some flexibility at lower NRE cost than a fully custom design.