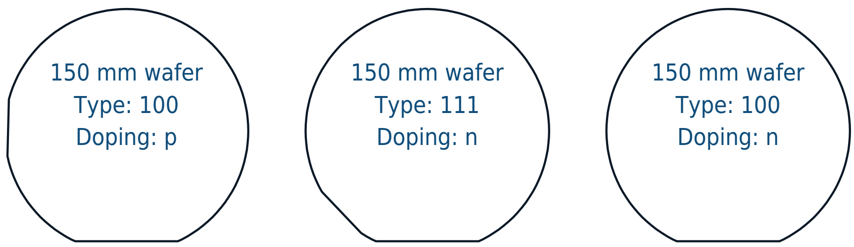
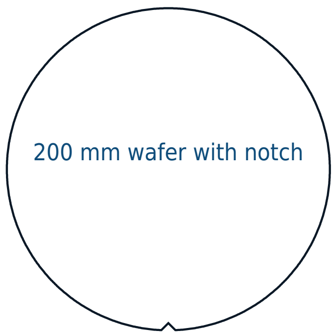
Semiconductor Technology from A to Z

Wafer Fabrication

Wafer Slicing and Surface Finishing

The single-crystal rod is first ground down to the desired diameter and then, depending on crystal orientation and doping, given one or two flats. The larger flat is used to precisely align the wafers during production. The second flat identifies the wafer type (crystal orientation, p-/n-doping), but is not always present. For wafers 200 mm in diameter and larger, so-called notches are used instead of flats. These are tiny notches at the edge of the wafer that likewise allow the wafer to be aligned, but take up far less of the wafer's valuable surface area.





Sawing

Historically, the single-crystal rod was cut using an internal diameter (ID) saw, whose cutting edge is coated with diamond fragments. It cuts precisely, but only one wafer at a time, and up to 20 % of the crystal rod is lost to the thickness of the saw blade. Given today's rod diameters and wafer prices, this is no longer acceptable; the standard method is therefore wire sawing, in which several hundred wafers are cut from the rod in a single pass. A long wire, wetted with a slurry of silicon carbide grains and a carrier fluid such as glycol or oil, is guided over rotating rollers. The silicon crystal is lowered into the wire grid and thereby sliced into wafers. The wire moves back and forth at about 10 m/s and is typically 0.1–0.2 mm thick. Increasingly, instead of a slurry of loose grains, a wire with diamond grains fixed firmly into its surface is used. It cuts faster, produces less waste, and eliminates the need to dispose of spent slurry.

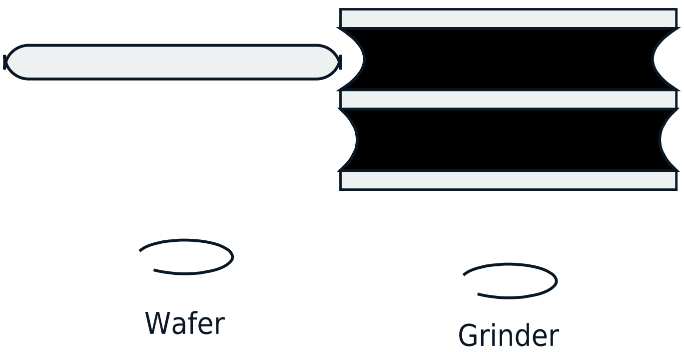
After sawing, the wafers have a roughened surface and, due to the mechanical stress, lattice damage within the crystal. To refine the surface, the wafers pass through several process steps.

Lapping

Using granular abrasives (e.g. aluminium oxide) on a rotating steel plate, 50 µm (0.05 mm) of the wafer surface is removed. The grain size is reduced in stages, but the surface is once again damaged by the mechanical treatment. The flatness after lapping is about 2 µm.

Rounding the wafer edge

In later processes, the wafers must not have any sharp edges, since deposited layers could otherwise flake off. For this reason, the edge of the wafers is rounded off using a diamond grinding tool.



Etching

In a dip-etch step using a mixture of hydrofluoric, acetic, and nitric acid, a further 50 µm is removed. Since this is a chemical process, the surface is not damaged. Crystal defects are finally eliminated.

Polishing

This is the final step toward the finished wafer. At the end of the polishing step, the wafers have a remaining unevenness of less than 3 nm (0.000003 mm). For this, the wafers are treated with a mixture of sodium hydroxide solution (NaOH), water, and silicon dioxide particles. The silicon dioxide removes a further 5 µm from the wafer surface, while the sodium hydroxide removes oxide and eliminates processing marks left by the silicon dioxide particles.

This is followed by a final cleaning and a measurement of each individual wafer for flatness, thickness, and particles. A considerable proportion of wafers subsequently also receive an epitaxial layer: a thin, especially pure, and precisely doped layer of silicon grown onto the polished surface. The actual devices are then formed in this layer, while the wafer beneath serves only as a carrier.

Historical Development of Wafer Size

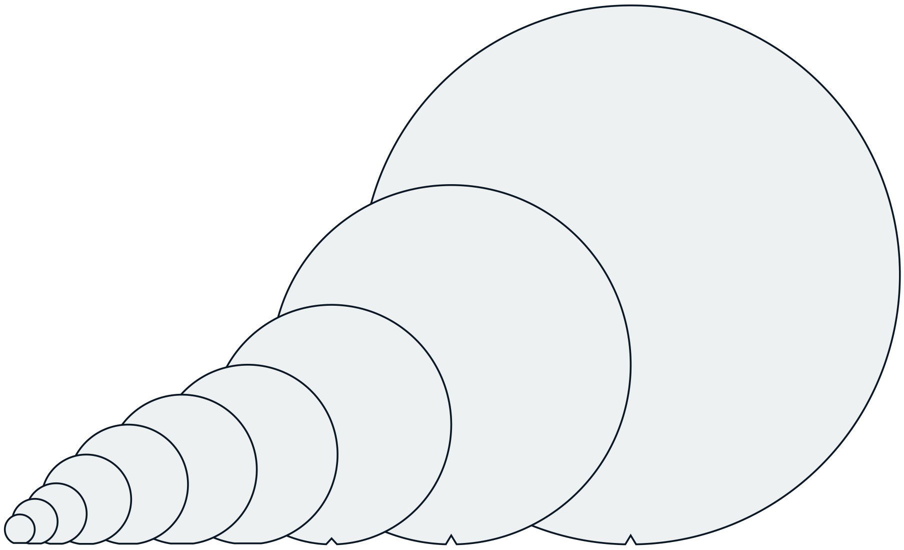
The manufacture of integrated circuits on silicon wafers began in the mid-1960s using wafers with a diameter of 25 mm. Since then, the diameter has grown in steps; since the late 1990s, the 300 mm wafer has been the largest format used in volume production. Its area is roughly 140 times that of the first 25 mm wafers.

With larger wafers, throughput in chip manufacturing increases considerably, allowing manufacturing costs to be reduced accordingly. For example, at the same feature size, more than twice as many chips can be produced on a 300 mm wafer as on a 200 mm wafer.

Typical wafer data:

Type [mm]	Diameter [mm]	Thickness [µm]	Primary flat [mm]	Bow [µm]
150	150 ± 0.5	~700	55 - 60	25
200	200 ± 0.5	~800	*Notch*	35
300	300 ± 0.5	~900	*Notch*	45

Overview of wafer sizes: 25, 38, 51, 75, 100, 125, 150, 200, 300, 450 [mm] (to scale)



The Step to 450 mm That Never Happened

The progression was supposed to continue with 450 mm. Around 2008, several major manufacturers and equipment suppliers joined forces in a shared program; initial equipment and test wafers were produced, and the transition was announced for the early 2010s. It never happened: the program was shut down in the mid-2010s, and 300 mm has remained the largest format to this day.

The reasons for this already lie in the technical difficulties that were being tackled at the time:

- Bow increases with diameter. To prevent stacked wafers from touching each other during transport, spacings, supports, and grippers would have had to be redesigned.
- Film stresses deform a large wafer more easily. It cannot simply be made thicker, since material costs and natural frequency work against this.
- The larger area also has to be processed. Compared with 300 mm, the cost per square centimeter would have had to fall by a factor of 2.25 for the economics to work out at all.
- A 450 mm crystal takes more than twice as long to grow. During this time, the probability of defects being incorporated into the lattice also increases.
- Almost every piece of equipment on the production line would have had to be redeveloped – at an investment level that individual manufacturers could no longer bear on their own.

The decisive point, however, was an economic one. The benefit of a larger wafer lies in spreading the fixed cost per piece of equipment over more chips. This advantage becomes smaller the more expensive the individual piece of equipment becomes – and lithography equipment became dramatically more expensive during the same period. The effort required for the transition would therefore have increased, while the return from it decreased. Instead, the industry directed its investments toward smaller feature sizes and the third dimension: more devices per unit area rather than more area per wafer.

Why Are Wafers Round?

The question often arises as to why wafers are round, since microchips are, after all, rectangular. This inevitably results in wasted area on the wafer – area where no complete chips fit, and which must ultimately be discarded at the end of semiconductor manufacturing.

Having explained the two manufacturing processes - the crystal growth process and zone pulling - this question can easily be answered.

A silicon wafer for microchip manufacturing must be a single crystal. This is only possible with the processes mentioned, and these inherently produce a circular shape.

Even though it would be technically possible to subsequently shape the round silicon crystals into an angular form (e. g. by sawing), the round shape of silicon wafers nevertheless offers several advantages despite the rectangular microchips.

- Straightening the round silicon rods would place additional stress on the material and would inevitably lead to crystal defects that would affect chip quality.
- Round wafers are considerably more robust. Angular wafers could hardly be transported and processed without damage.
- Uniform processing during chip manufacturing using radially symmetric processes (CMP, spin-on, etching) is considerably simpler.
- A narrow edge region would always have to be discarded even with rectangular wafers, since the wafers must be held during processing. Deposited layers would flake off and generate additional particles if they extended all the way to the outermost edge.

As wafer size increases, the amount of wasted area also continues to decrease.

Rectangular wafers, on the other hand, are found in the manufacture of solar cells. Polycrystalline wafers are mostly used here, which can be cast into rectangular shapes. Manufacturing is comparatively simple, so angular wafers can be processed as well. The corners are usually additionally chamfered. For today's common single-crystal solar cells, it is exactly the other way around: they are made from crystals pulled in round form, which are trimmed to a square shape before sawing – with rounded corners, because cutting away the remaining edge would cost more material than the gain in area would be worth.